PERFORMANCE ESTIMATION OF LARGE AREA NANOWIRES

A Thesis
Presented to
The Academic Faculty

By

Keval Prakash Kamdar

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PERFORMANCE ESTIMATION OF LARGE AREA NANOWIRES

Approved by:

Dr. Arijit Raychowdhury, Advisor
Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Sung-Kyu Lim
Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Asif Khan
Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: April 22, 2019

Study hard what interests you the most in the most undisciplined, irreverent and original manner possible.

Richard P. Feynman

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I would like to begin by expressing my sincere gratitude to my advisor, Dr. Arijit Raychowdhury for his patient and focused guidance to me throughout the course of my Masters. I started as a graduate student under him in Spring 2018 and I cannot thank him enough for his help to me throughout this important phase in my life. His knowledge on the execution of device and circuit design speaks volumes and I am astonished by his calm and composure couple with the ability to work in areas which require a lot of breadth. His class and his talks inspired me to take up devices, something I never thought I would have been able to do.

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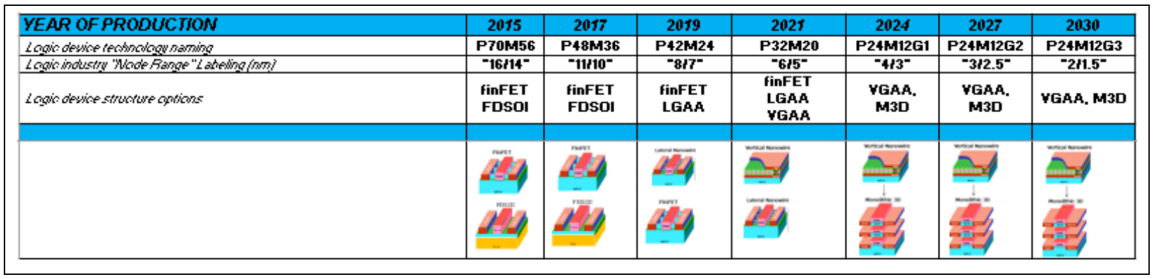
SUMMARY

The focus of the thesis is to extensively model high-performance nanowires, develop Verilog A models of the devices and then simulate them using SPICE to estimate their power-performance trade-offs. Once the device models are created, they will be used in circuits which will have realistic interconnects with necessary parasitic resistance and impedance (inductance and capacitance) and simulated for prototypical digital and mixed signal designs. The device and the circuit simulation infrastructure will be developed in parallel. Synopsys Taurus and Medici will be used for 3D device modelling, Verilog A for circuit-compatible models, and Spice for circuit and system evaluation.

CHAPTER 1

INTRODUCTION AND BACKGROUND

The end of the Moore's law[1] has been predicted now and again. And every time that this happens, new technologies have come up to dispell these fears. We moved on from MOSFETs with PolySilicon Gates in the 65nm node to High-K Metal Gate in the 45nm node to using sophisticated FinFETs in the 7nm technology node. But as this roadmap continues, many new questions continue to arise? How long will we able to scale down with the existing tri-gate FinFETs? If not, then what will happen after FinFETS? Although using multigate devices actually leads to a much better device and circuit performance, they are a challenge to execute from the technology and the process point of view. [2] explains various architectures for transistors down the road discussing the advantages and disadvantages of each of them. Lastly it also discusses the question of how many gates will be required to sustain a continuous increase in performance to sustain the ITRS roadmap and eventually the Moore's law. One of the best candidates to replace the existing FinFETs to support the scaling down of the devices with the same or better performance is a Gate All Around Nanowire FET. Once, the high performance devices have been designed, the application



YEAR OF PRODUCTION	2015	2017	2019	2021	2024	2027	2030
Logic device technology naming	P70M56	P48M36	P42M24	P32M20	P24M12G1	P24M12G2	P24M12G3
Logic industry "Node Range" Labeling (nm)	"16/14"	"11/10"	"8/7"	"6/5"	"4/3"	"3/2.5"	"2/1.5"
Logic device structure options	finFET FDSOI	finFET FDSOI	finFET LGAA	finFET LGAA ¥GAA	¥GAA, M3D	¥GAA, M3D	¥GAA, M3D

Figure MM3: Transistor structure roadmap: FDSOI, finFET, lateral nanowire, vertical nanowire, and monolithic 3D.

Figure 1.1: Latest ITRS Roadmap for Semiconductors

of the devices is the next question that needs to be answered? We focus our work on Large Area Electronics in general. This paradigm of Large Area Electronics is used as

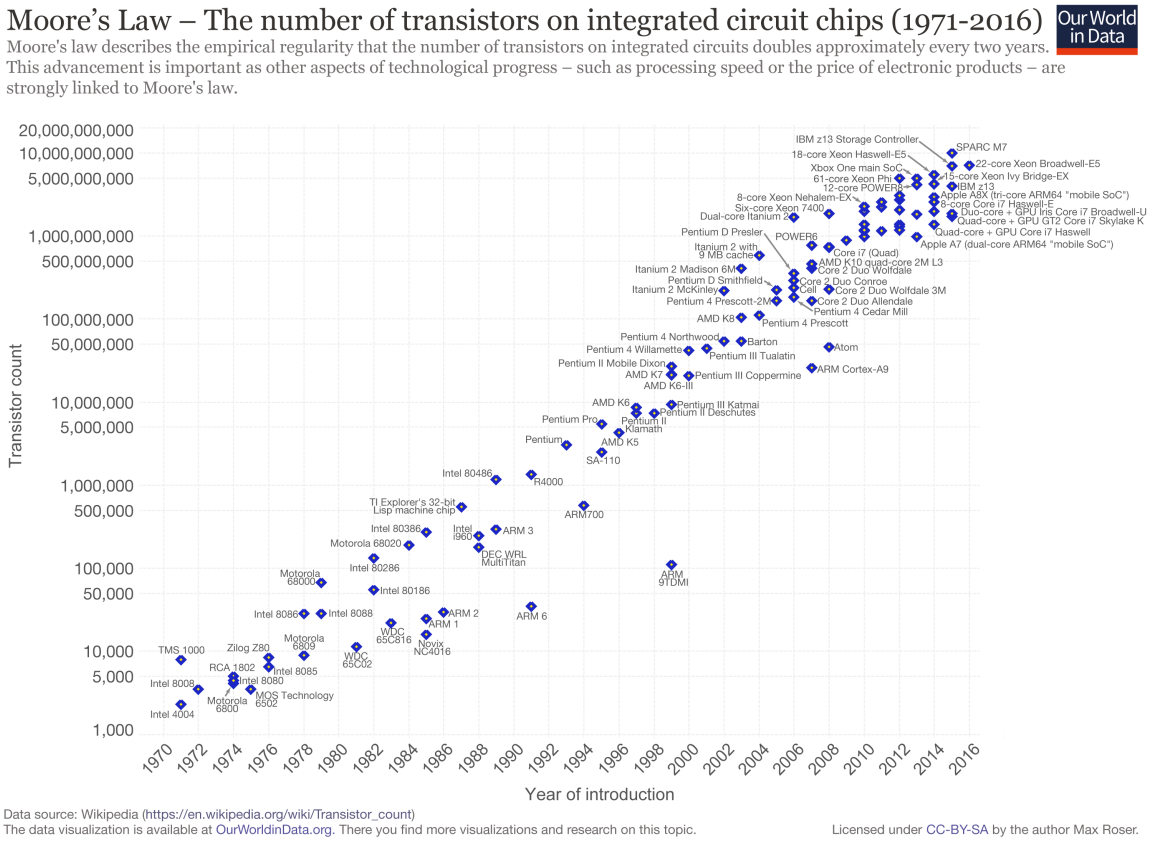


Figure 1.2: Moore's Law for Semiconductors[3]

a next generation of technology to make Human Computer Interaction more achievable. These devices rely on inputs that are implicit with our interactions from the environment rather than actively providing inputs to the system. This requires a large number of sensors dispersed in the environment that basically detect implicit signals from humans and other sensors for some signal processing. [4]

Combining these two efforts into one, this thesis mainly focuses on developing large area electronics using state of the art nanowire devices which have very high performance coupled with a complete photolithography-free manufacturing technology. Many researchers have focused on the Gate All Around devices [5], although most of the devices that have been manufactured using a lithographical process which can get extremely expensive as the technology node scales down. The problem that we are trying to tackle is to manufacture electronics which can be dispersed in high amounts in the form of integrated circuits

in different wireless sensors but at the same time also have a high performance compared to traditional large area devices. Plotting a graph of existing devices with Performance on X axis and the scale of production on Y axis, most of the devices today fall in either the second or the fourth quadrant with high performance and low scalability in terms of production or can be produced in really high volume albeit with a poor performance.

At Georgia Institute of Technology, Professor Eric Vogel's group is responsible for making nanowire transistors that can be manufactured in high volumes sustaining the performance of these devices, which can be used for latest large area electronic applications. At ECE, we were responsible for simultaneously developing simulation models of these transistors using industry standard device simulators, creating digital circuits from these nanowire device models and then analyzing the performance of this circuits. Adding interconnects to these circuits and seeing the behaviour of parasitics on the performance of digital circuits is also important.

All in all, the focus of the thesis is to extensively model high-performance nanowires, develop Verilog A models of the devices and then simulate them using SPECTRE to estimate their power-performance trade-offs. Once the device models were created, they were used in circuits which will have realistic interconnects with necessary parasitic resistance and impedance (inductance and capacitance) and simulated for prototypical digital and mixed signal designs. The device and the circuit simulation infrastructure was developed in parallel. Synopsys Sentaurus TCAD has been used for 3D device modelling, Verilog A for circuit-compatible models, and SPECTRE for circuit and system evaluation. Three major tasks of consequence as a part of this work have been described below:

- ***Device Simulation Research***: Gate All Around FETs, called Nanowires have been implemented using Sentaurus TCAD. Geometries were examined and created. Meshing structures were generated using a right balance which would make the accuracy right and the runtime faster. Appropriate physical models to account for mobility, scattering and surface roughness were added. Devices are then sweeped to obtain

appropriate current voltage characteristics, using suitable Poisson, Hole, Electron and QuantumPotential Equations.

- ***Circuit Simulation Infrastructure***: After the PMOS and the NMOS tube devices were simulated, an infrastructure was developed. The infrastructure which was implemented in python. It would start with parsing through the log files of the device simulator, to create a table model for the circuit simulator. The table model was instantiated in Verilog-A to implement simple versions of NMOS and PMOS Nanowire Transistors. After that an input was taken from the user and then a netlist was created in python. The spectre netlist is customizable so as to do a DC or Transient Analysis.

- ***Circuit Simulation Research***: Once the Verilog-A models have been instantiated, different circuits according to the netlist input provided by the user are created. These are circuits that are Figure-of-Merit Circuits that have been used in the industry for basic technology prototyping. Inverters, CMOS NAND, CMOS NOR, Ring Oscillators have been tested. Once the circuits are tested with ideal interconnects, realistic interconnects have been added to them keeping in mind the large area electronics application of such circuits.

The subsequent part of the Introduction will introduce the users to some background on transistors, use-case and requirements of Gate All Around devices, the relevance of Implemented Nanowire devices. Circuit simulation background has also been provided to elucidate things for the reader. The problem statement has also been motivated.

1.1 Device Simulation Background and Problem Statement

As the technology node scales down several effects are observed in transistors. These effects can be easily neglected for first order analysis. But to get a greater accuracy over the transistor operation and understand the current scaling roadmap, we cannot neglect these effects. Any new technology node that comes out, focuses on improving the transistor by 2 important aspects.

- Electrostatics of Device.
- Transport through the Channel.

As devices progressed down the ITRS roadmap, they strived to improve one or both of these parameters and we are at FinFETs today. Transistors today operate have 3 regions of operation: Cutoff, Linear and Saturation. Operation of transistors in any of the three regions is controlled by the Gate to Source Voltage V_{gs}, the Drain to Source Voltage V_{ds} and the Threshold Voltage of the device V_t. The I-V characteristics of the device are referenced to the threshold voltage of the device which is set during the fabrication. In the cutoff the transistor does not conduct, whereas in saturation mode, the transistor behaves as a perfect current source. The current in the cutoff region is approximately equal to the off current of the device. The current in linear region is linearly dependent on the resistance of the device, whereas in the saturation region the current is constant barring some channel length modulation effects where current increases as V_{ds} increases. As the devices were scaled, the current, voltage and other parameters scaled with them. Scaling theory does not take into account what happens when the device channel length reduces. Big device models help to attain simplicity but a greater modification of the parameters is important to accurately model the small length effects. Most of the small device effects introduce a change in the threshold voltage of the device and hence the electrostatics are affected.

Short Channel effects[6] start becoming important when the device channel length starts to go below 2μm or so. The main result is that the threshold voltage is reduced below the

value found by long channel analysis. The origin of the short channel reduction of the threshold voltage is due to the fact that the gate voltage (and hence, the threshold voltage) does not support all of the bulk charge with an area of WL underneath the gate. Rather, some of the depletion charge at the drain and source sides of the channel is automatically induced by the ionized dopants that form the pn junctions. This says that the bulk charge term in V_t overestimates the size of this contribution. Figure 1.3 explains the phenomenon

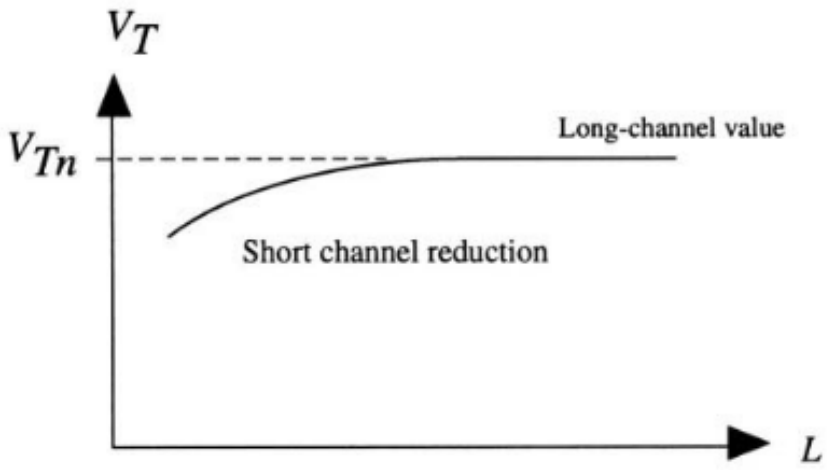


Figure 1.3: Short Channel Effects in Transistors [6]

of Short Channel Effects and its reduction of Reduction of Threshold voltage vs Channel length. Transition from Planar MOSFETs to Double Gated devices to FinFETs ensured that the device is controlled by the gate more than the source and the drain. This is because when you have more gates you have a higher probability of depleting the charge in the bulk or the body by the gate itself rather than drain or the source. So FinFETs nowadays aren't controlled at all by body biasing effects. Gate All Around MOSFETs are the ultimate solution to this Short Channel Effect problem that is just one of the problems with smaller devices. Gate All around devices ensure that the charge depletion in the channel is to the maximum caused by the Gate itself. And also since the channel has been covered on all 4 sides by the gate, the gate can more efficiently control the flow of charge inside the channel and consequently the current can also be controlled better. This thesis focuses on

the development of simulation infrastructure for the actual nanowire models that are being implemented. The motivation is to use these high performance gate all around devices for large area electronics.

The concept of large area electronics requires that the sensors should not only be capable of sensing environmental signals, perform some simple calculations on the acquired signal, wirelessly transmit the signal to the computation unit but should be widely distributed over a large area to provide high resolution data or they should be located in difficult to access tight spaces. Sensors can be definitely printed today but to enable wireless communication as well as lower power dissipation, high performance active devices are required. These devices are added in a hybrid fashion which limits the throughput and the dispersibility. As mentioned earlier, to make devices in the first quadrant i.e. manufacturing high volume of high performance devices is a tedious task. Current fabrication schemes are limited by the limited by the physicochemical process that are not adequate enough to fulfill the above manufacturing requirements. For example: Slow rates of near equilibrium crystal growth and top down lithographic feature definition affect the maturity and the application of wafer based methods for such high volume manufacturing. Manufacturing of the devices that are simulated in this work are a result of a complete modular manufacturing system with the ability to do complete bottom-up photolithography-free fabrication process of nanoscale electronics and adaptive interconnection of discrete plug and play devices to form functional circuitry. Bottom up fabrication imparts the devices the ability to create a seperate source, drain and channel as well as a perfectly self aligned gate stack. Simulations in Section 2 show that the devices are capable of achieving performance as well as operate at a low voltage. Cost and time associated with top-down lithography is eliminated to allow an enormous scale fabrication of these devices. The final motive on the fabrication side is to manufacture plug and play electronic devices where they can be just spread out on a substrate and their connection can be envisioned using some software help to make different circuits maximizing the device locations and the circuit efficiency.

1.2 Circuit Simulation Infrastructure and Research

As mentioned in the previous section for device simulation, the main motive for these devices is to make plug and play circuits that can be assembled anywhere to make state of the art wireless sensor nodes. The devices that have to be built are simulated in the device simulator. The device simulator log files are parsed using python to obtain arrays of different simulation results like drain current, gate voltage and so on. All of the circuit simulation can be done interactively by visually launching the tool, but creation of a scripted infrastructure to plot the results and view them enables us to reduce the runtime for simulation and analyze things faster. Once the different log files have been parsed, they are plotted to obtain the curves for the device simulations (I_d-V_{gs}, I_d-V_{ds}). Also the data obtained from these files is transformed into a table model suitable for Verilog-A. Verilog-A offers a very powerful insight into how to model devices for doing prototypes for digital and mixed signal circuits. Table Model function inbuilt into the Verilog-A Language creates and imports a look-up table as an operational form of the transistor in question. SPICE Models are not needed. The Look-up table is sufficient for a full-fledged operation of the device. After the look up tables have been setup, simple NMOS and PMOS were simulated. Circuit simulators run much faster as compared to traditional device simulators. In addition to this, the novelty of the simulator lies in the fact that it requires only two isolines of I_d - V_{ds} - V_{gs} data at a minimum to operate. It can interpolate and extrapolate the current values for the voltages not in the table with a linear, quadratic or a cubic option with an option to do it at both ends of the curve. A netlist is created taking an input from the user whilst also specifying whether it's a DC or a transient simulation.

The problem is motivated by the background to solve basic circuit research problems associated with new kinds of devices. As with any new hardware technology, the challenge is to get the circuit operations functionally correct. Simulations of standalone transistors was implemented for different results. After the transistors were implemented, basic fun-

damental figure of merit circuits were used. Some of these circuits are as follows:

- CMOS Inverter: The first circuit to be tested in any new logic technology which gives an output opposite to the input logic level.
- CMOS NAND Gate: One of the two universal gates which can be used to implement any logic circuit. It's output is low when both inputs are high.
- CMOS NOR Gate: This gate is a second universal gate which outputs logic high when both inputs are at logic low.
- Full Adder: A complex 3-input 1 bit adder which has the capability to add carry signals that are propagated from the previous stages as well. Functional verification of the full adder is important before proceeding to implement big logic blocks in any technology.
- Ring Oscillator: Ring Oscillator is a chain of odd number of inverters connected back to back with the output of the last stage going back to the input of the first stage. Understanding the frequency of oscillations and device variation effects on a ring oscillator provides a lot of new insight on how the technology is expected to perform on bigger blocks.
- Inverter with Fanout-4: As the switching speeds of the inverter are largely dependent on the output load capacitance, testing an inverter gate which has a fanout of 4 gates (an industry standard test circuit) gives a great insight as to how load capacitnace is important to circuit design.
- 6-T SRAM Bitcell: A 6-Transistor SRAM Bitcell analyzed for it's verification and Static Noise margin butterfly curves are characterised as for any new device technology.

1.3 Circuit Design Analysis

After the circuits have been designed, they need to be verified for the functionality. Nanowires being Gate All around devices are capable of giving very good device electrostatics But since the length of the device is greater than the width, it can lead to insufficient currents for some digital application. An important consideration which comes into play here is deciding the number of tubes that should be used in the pull-up or the pull-down section of a static CMOS circuit. More the number of NMOS tubes, more will be the drive strength the pull-down network and hence the circuit will take lesser time to switch to a logic low level. On the other hand, more number of PMOS Nanowires will make the pull-up network stronger and hence the time taken for the circuit to switch from a logic low to a logic high level will be lesser resulting in skewed circuits. An example of VTC curves in case of skewed responses is shown in thhe figure below. A more thorough understanding of skewing is explained in the circuits section.

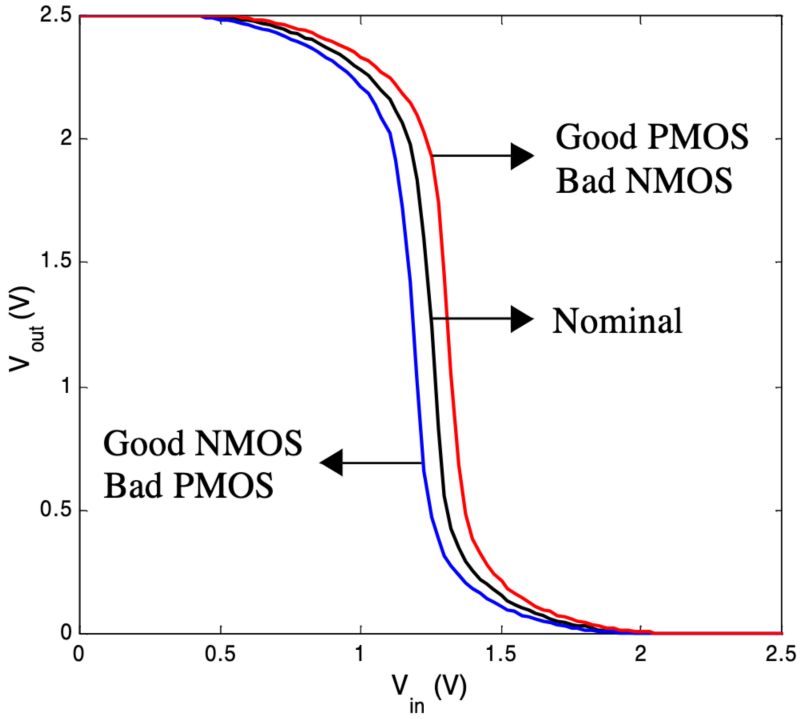


Figure 1.4: Skewed Inverter DC Response [6]

Once, the netlist of the inverter has been setup, measurements have been taken for different inverter characteristics looking at the DC or the Transient Response of the Inverter. After the CMOS Inverter the different Static CMOS Logic Gates like the NAND, NOR have been tested. Functional verification of these different logic circuits is an important part of any new logic technology.

Interconnects in the circuit design analysis offer a much better perspective of how things will look when the technologies scale down. We are going to be limited by the interconnect dimensions because they do not scale as well as the transistor dimensions do. Due to this, in the latest technology nodes, they are the bottlenecks that can hinder performance. Testing out our circuits we start with a 1fF load capacitance at the output, simulate and plot the outputs. To get an idea of more realistic interconnects, we lump together 5 models of capacitance into one output capacitance and determine the same results. Plug and Play electronics, the ones we intend to develop and model are limited by the interconnect parasitics due to the technology node they are operating on coupled with the distance between the devices. So analysis of Interconnect Resistance and Capacitance plays a major role in concluding the testing of the Circuits.

The subsequent sections explain each of the aspect of this work in detail viz. the devices and the circuits. Devices section explains the device geometries, physical models. It finally explains the meshing strategies, simulation model infrastructure and lists down the evaluation for all the different PMOS and NMOS Nanowire devices. Circuits Section explains the circuit construction, their ideal working without any interconnect resistance and capacitances, plots the responses and also summarizes some important switching numbers. Interconnects have been explored thereafter varying the interconnect distance between the devices and circuits and thereby plotting the distance vs switching speeds to understand how interconnects are going to affect the performance.

CHAPTER 2

DEVICE SIMULATION

This section will talk in detail about the device simulations with respect to the large area devices. Device Simulation is the first step in the 3 stage flow which involves circuit simulation and Benchmarking against a standard technology as well. Device simulations were essential to understand the modelling of the device from the simple geometries and the doping characteristics which are used for manufacturing the devices. Manufacturing the actual devices physically takes a lot of iterative effort along with the abundance of chemistry and material science that goes along with it. Simulations on the other hand will be completed comparatively faster. So these simulations serve as a stepping stones to achieving the perfect device from devices that we have today. Our device simulations are implemented using standard TCAD industry tool from Synopsys called the Synopsys Sentaurus TCAD. This section explains the Tools and the tool flow for Sentaurus TCAD used for the thesis, the 6 devices that I have explored for my thesis, their device simulation strategies, explanation of the various mathematical and the physical models used for solving the devices and the evaluation of the simulator results for all our devices.

2.1 Tools for the Device Simulation

This section will talk about the tools used for the Device Simulation. As mentioned earlier, Synopsys Sentaurus TCAD Suite [7],[8],[9] is used for device simulation and evaluations. TCAD stands for Technology Computer Aided Design. It refers to the process of running computer simulations to develop new semiconductor processing technologies and devices. Sentaurus TCAD suite offers comprehensive modelling tools for simulating new process technologies, generating new device geometries and simulating high end physics models for device simulations. It also offers a relatively easy to use GUI to aid the new users. These TCAD tools have been used in this project simultaneously along with the manufacturing process to develop new devices and extract their electrical parameters. The tools can be run interactively using the GUI or using batch scripts. The flow of the tool usage is described in the figure 2.1 below:

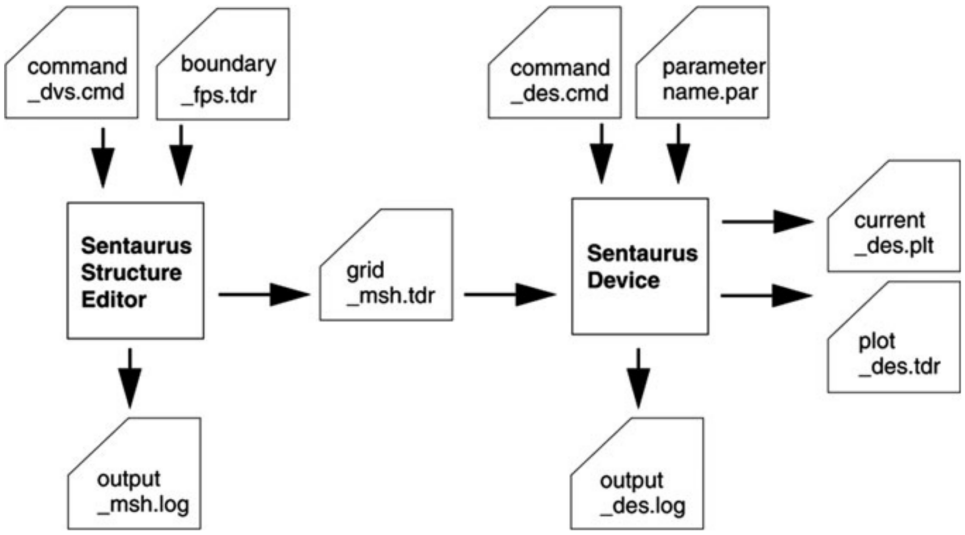


Figure 2.1: *Toolflow with device simulation using Sentaurus Device.[8]*

The function of each of the block in the figure 2.2 is summarized.

- **Sentaurus Device Editor (SDE)**: Sentaurus Structure Editor is a tool in the TCAD suite which is used for building structures of the devices. SDE is equipped to draw

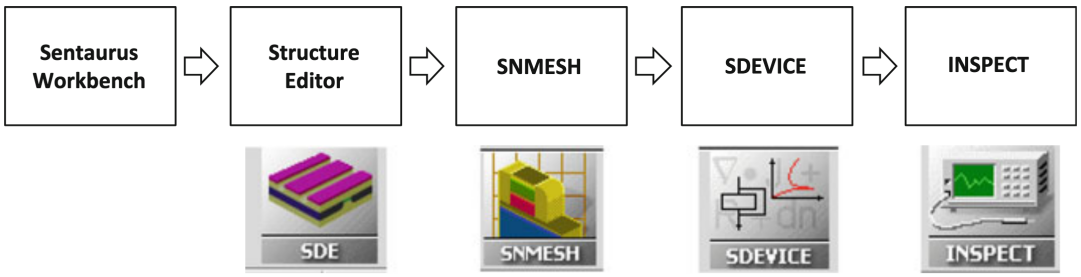


Figure 2.2: *Basic Process flowchart of the simulation tools using Synopsys Sentaurus TCAD [10]*

2D or 3D diagrams for these devices. It can be used to view devices at the same time that they are being built. The visualization tool along with SDE is such that you can turn off certain layers of the devices that you are building so that it gives you an efficient view of the geometry that you are building. Nanowire devices are built using cylinders composed of silicon representing the 3 regions. Oxide is deposited on top of the channel region. All the dimensions like length, thickness, metal gate workfunction, operating voltages can be parameterized.

- **Sentaurus Mesh**: Sentaurus Mesh refers to the points on the device where the mathematical equations can be solved, where the density can be self defined. The location with denser mesh can better reflect the variation of physical properties of this area, such as potential gradient, electric field gradient, and carrier concentration gradient, but the denser the mesh it can lead to more runtime for the simulation.

- **Sentaurus Device**: Sentaurus device is a general purpose simulation tool that is used for simulating the device geometries using various physical and mathematical models to plot current voltage characteristics.

- **Sentaurus Visual**: Sentaurus Visual tool is the advanced visualization software for TCAD data analysis. It is equipped with rich graphics capabilities for interactive composition of X–Y curves and 2D/3D TCAD device structures and device electrical and physical properties.

The Sentaurus Structure editor takes in the dimensions, doping and the boundary files as input. It generates a mesh file that has an extension **"_msh.tdr"**. This mesh file is taken as input by the Sentaurus device. The Sentaurus device also takes other inputs like the command file and the parameter file. The command file basically has all the constraints, models and the ranges of voltages to simulate the device. The parameter file includes the properties for new materials developed and used in the simulation that are not a part of the Sentaurus models by default. The Simulation produces a **".plt"** file which has the sweeped current voltage values. This file is used by Sentaurus Visual to view the current voltage plots. The view of the GUI which is a part of the Sentaurus Structure Editor has been shown in figure **??**. It offers a very comprehensive toolbox for creating 3D shapes which is pretty intuitive to the user. It also has the capability to isometrically rotate the geometries created and change the material used for construction.

2.2 Devices in Detail

This section will describe the type of devices that we worked on. The devices are Nanowires which were designed using a printing method rather than the traditional lithography. The name nanowire actually comes from the fact that the length is greater than width of the device. A nanowire is actually cylindrical MOSFET that have source, drain and channel. One of the major advantages of using a Nanowires is actually the fact that a nanowire is a Gate All Around device. Transistors over the years have two major characteristics that have improved every generation the transistor has gotten better, viz. Transport and Electrostatics. We moved from Double gated devices to Tri-gated FinFETs for the reason, that since FinFET is a tri-gated device it will give us a greater charge control over the channel. Gate All Around (GAA) Devices are the next in line to take over from FinFETs. The Nanowires, being GAA Devices, will enable the wrapped around gate to have a greater charge control over the channel, hence improved electrostatics. A greater charge control will eventually lead to a smaller amount of gate voltage required to deplete the channel. This reduction in the gate voltage to deplete a channel translates into a reduction of threshold voltage of the device as compared to a conventional MOSFET. A lower threshold voltage will lead to a lesser delay in turning on the device and finally leads to a higher performance as compared to conventional planar MOSFETs. The better transport of a GAA device results in a greater on saturation current and hence reduced resistance.

We look at 3 kinds of devices depending on the geometries and the alignment of the gate with the channel. Each device that we explored as a part of this thesis has its own challenges in the form of geometries and the doping. The devices have varying geometries and overlap behaviour. Furthermore, we have evaluated the NMOS (N-Channel MOSFET) and the PMOS (P-Channel MOSFET) transistors for each of the different device structures that we talk about. The three devices in decreasing order of sizes in our road-map have been listed below:

- Long Channel Long Terminal Device (PMOS & NMOS)
- Short Channel Long Terminal Device (PMOS & NMOS)
- Short Channel Short Terminal Device (PMOS & NMOS)

For a successful device simulation, a serious understanding all the various aspects of the device geometry, being able to incorporate that geometry in the Sentaurus Structure Editor is mandatory. Once, the geometries are incorporated, the problem of meshing comes from the background to the foreground. The implications of an incorrect mesh can be very problematic and will always lead to the failure of the device simulator convergence. Once, the mesh has been finalised, the actual device simulation comes into the picture. Sentaurus Device Simulator takes into account various physical models that are needed to be incorporated during solving of the device. Various mathematical modelling parameters have also been specified at this stage.

In the subsequent section, we explain the Short Channel Short Terminal NMOS Transistor in detail with respect to the geometry, the doping concentrations and their meshing parameters. I also explain the TCL script to get an intuitive understanding of the device construction with respect to the tool. Scripts used to run the physics inside a device simulator are also delineated and explained. After that, we basically draw comparisons to the Short Channel Short Terminal NMOS to contrast doping for a PMOS example and dimensions to contrast different devices.

2.2.1 Short Channel Short Terminal NMOS

This section talks about the short channel short terminal device (End Road Map device). To ease the process of understanding the devices, we have divided this section into various subsections, each of which explains a major step in the device simulation.

The Short Channel Short Terminal (SCST) device is actually the smallest devices in all the three device configurations and geometries that we have worked upon. The End Road-Map device is an all Silicon device. Source and Drain terminals along with the Channel are made out of Silicon. They are cylinders of Silicon stacked on top of each other. The gate in the SCST Device is actually self aligned on top of the channel. The source and the drain terminals are 500nm long with a diameter of 100nm. The oxide deposited on top is silicon dioxide SiO_2 with a relative permittivity of 3.9 F/m. The thickness of the deposited silicon dioxide is around 5nm. Eventually the gate is contacted on top of this silicon dioxide. The doping of the source and the drain is determined by whether it is a PMOS or an NMOS Transistor. For the PMOS Transistors, the drain and source are doped with Boron with a concentration of about $10^{20}cm^{-3}$. On the other hand, in case of the NMOS Transistors, the drain and the source are doped with Phosphorous having a concentration of about $10^{20}cm^{-3}$. The channel is maintained at the inherent intrinsic doping level for both the PMOS and the NMOS. The WorkFunction of the gate contacted on the top of the SiO_2 can be manipulated in the device simulator script to get a varying degree of control of the device threshold voltage. The self alignment of the gate over the channel leads to an easier analysis of the device in a simulator. A non aligned gate on the channel would lead to the device capacitance being dominated by the overlap parasitic capacitance rather than the junction capacitance. Also, the absence of the bulk or the body from the device leads to an altogether better gate control.

This section will try to explain the construction of the device and link the geometry with the implementation in the tool[8].

```
(sdegeo:create-cylinder (position 0 0 0.09) (position 0 0 -0.09) 0.05 "Silicon" "channel")
```

```
(sdegeo:create-cylinder (position 0 0 0.09) (position 0 0 0.59) 0.05 "Silicon" "drain")
(sdegeo:create-cylinder (position 0 0 -0.09) (position 0 0 -0.59) 0.05 "Silicon" "source")
(sdegeo:set-default-boolean "BAB")
(sdegeo:create-cylinder (position 0 0 -0.09) (position 0 0 0.09) 0.055 "SiO2" "oxide")
(sdedr:define-constant-profile "DrainDefinition" "PhosphorousActiveConcentration" 1e+20)
(sdedr:define-constant-profile-region "DrainPlacement" "DrainDefinition" "drain")
(sdedr:define-constant-profile "SourceDefinition" "PhosphorousActiveConcentration" 1e+20)
(sdedr:define-constant-profile-region "SourcePlacement" "SourceDefinition" "source")
```

Listing 2.1: Geometry and Doping Statements

The code listing 2.1 generates the geometry of the device through various TCL (Tool Command Language) commands. Cylinders are defined for each of the three sections: Source, Drain and the Channel, using the **"sdegeo"** command. The argument 'position' will define the X, Y and the Z co-ordinates of the 2 circular faces of the cylinders. These arguments are followed by the radius and material which is used to construct them. The dielectric constant and other properties of the material are defined in models for the Sentaurus Structure Editor. The Old replaces New overlap behaviour defined by the command **"sdegeo: set-default-boolean"** ensures that the properties of the Silicon channel are not clouded by the SiO_2 on top of it. The next 2 commands aim at defining a Boron doping concentration for the source and the channel. These doping definition statements will change to Boron from Phosphorous currently to reflect a PMOS device. The words constant profile indicate that the regions are **uniformly** doped with the given carrier concentration.

```
(sdegeo:define-contact-set "gate" 4 (color:rgb 1 0 0 ) "##")
(sdegeo:define-contact-set "drain" 4 (color:rgb 0 1 0 ) "<><>")
(sdegeo:define-contact-set "source" 4 (color:rgb 0 0 1 ) "[] []")
(sdegeo:set-current-contact-set "gate")
(sdegeo:define-3d-contact (list (car (find-face-id (position 0.055 0.0 0)))) "gate")
(sdegeo:set-current-contact-set "drain")
(sdegeo:define-3d-contact (list (car (find-face-id (position 0.0 0.0 0.59)))) "drain")
(sdegeo:set-current-contact-set "source")
(sdegeo:define-3d-contact (list (car (find-face-id (position 0.0 0.0 -0.59)))) "source")
```

Listing 2.2: Definition of Contacts

The code listing 2.2 aims at defining the 3 contacts (Gate, Drain and Source). It also assigns the contact to the respective faces of the nanowire geometry. After the contacts have been assigned, the meshes are to be developed. The meshes are to be defined in a way so as to make the device simulator converge. The first step is to make a mesh around the entire device. In our case, since the entire device is of silicon, we make the first mesh on the basis of the material with 0.3 units as the maximum element size and 0.1 units as the minimum element size in all the 3 directions. A rule of thumb is that the channel needs to be evaluated properly as it is a region where the majority of carriers interact and most of the device action happens. So, we define a cuboidal reference window housing our channel. The fact that we are going to place an even denser mesh in the channel along with the global device level mesh we defined above makes it imperative for us to define a multi-box placement strategy. The steps following the multi-box placement infer the placement of the channel mesh in co-existence with the device mesh using functional arguments to refine the mesh functions like minimum and maximum element sizes, doping gradient and so on. The device model is then saved and the mesh is built using the **"sde: build-mesh"** command which generates a mesh file which is used in the device simulator to solve the physics of the device. This is explained in the code frame 2.3.

```
(sdedr:define-refinement-size "SiliconDefinition" 0.3 0.3 0.3 0.1 0.1 0.1 )
(sdedr:define-refinement-placement "SiliconPlacement" "SiliconDefinition" (list "material"
    "Silicon" ) )
(sdedr:define-refeval-window "Channel_Reference" "Cuboid" (position 0.05 0.05 0.09) (
    position -0.05 -0.05 -0.09))
(sdedr:define-multibox-size "MultiboxDefinition_1" 0.01 0.01 0.01 0.01 0.01 0.01 0.01 0.01
    0.01 )
(sdedr:define-multibox-placement "MultiboxPlacement_1" "MultiboxDefinition_1" "
    Channel_Reference" )
(sdedr:define-refinement-size "Channel_Mesh" 0.3 0.3 0.3 0.1 0.1 0.1 )
(sdedr:define-refinement-placement "Channel_Mesh_Placement_" "Channel_Mesh" (list "window"
    "Channel_Reference" ) )
```

```
(sdedr:define-refinement-function "Channel_Mesh" "DopingConcentration" "MaxTransDiff" 1)
(sde:save-model "ShortChannel_ShortTerminal_NMOS")
(sde:build-mesh "ShortChannel_ShortTerminal_NMOS")
```

Listing 2.3: Meshing Statements

Figures 2.3 and 2.4 show the Short Channel Short Terminal NMOS and its mesh to get an understanding of how the meshes look.

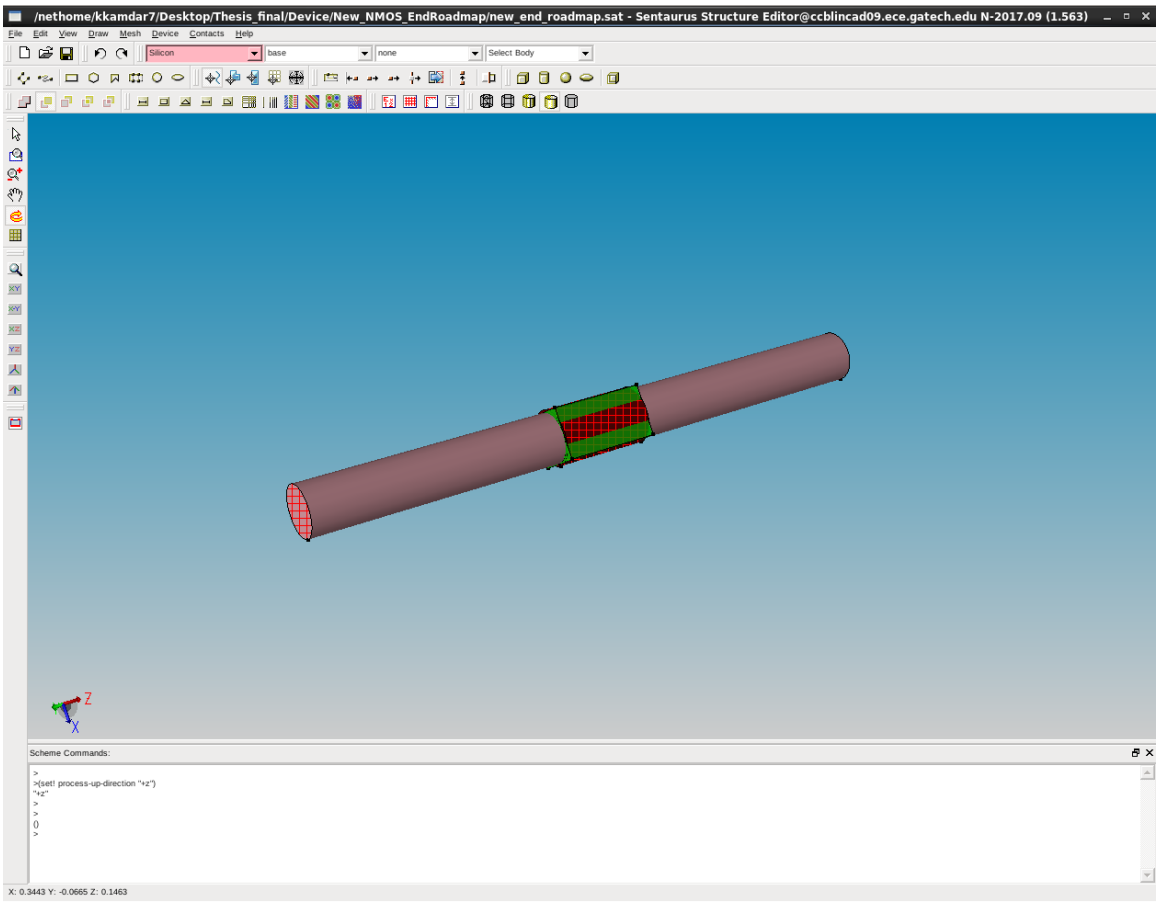


Figure 2.3: *Short Channel Short Terminal NMOS Geometry In the tool. [7]*

Figure 2.5a shows the geometry of the NMOS device that was simulated with the red color representing an N type region.

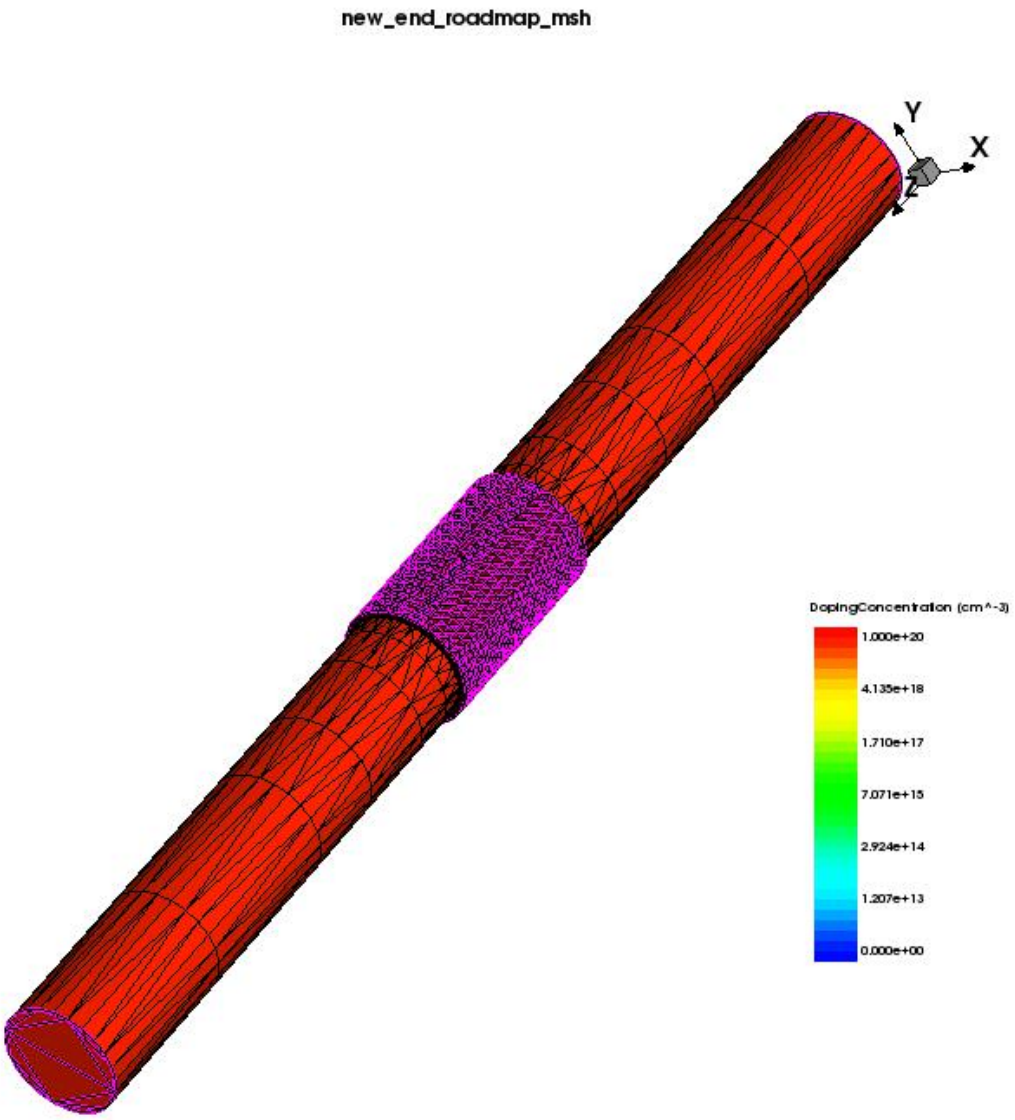
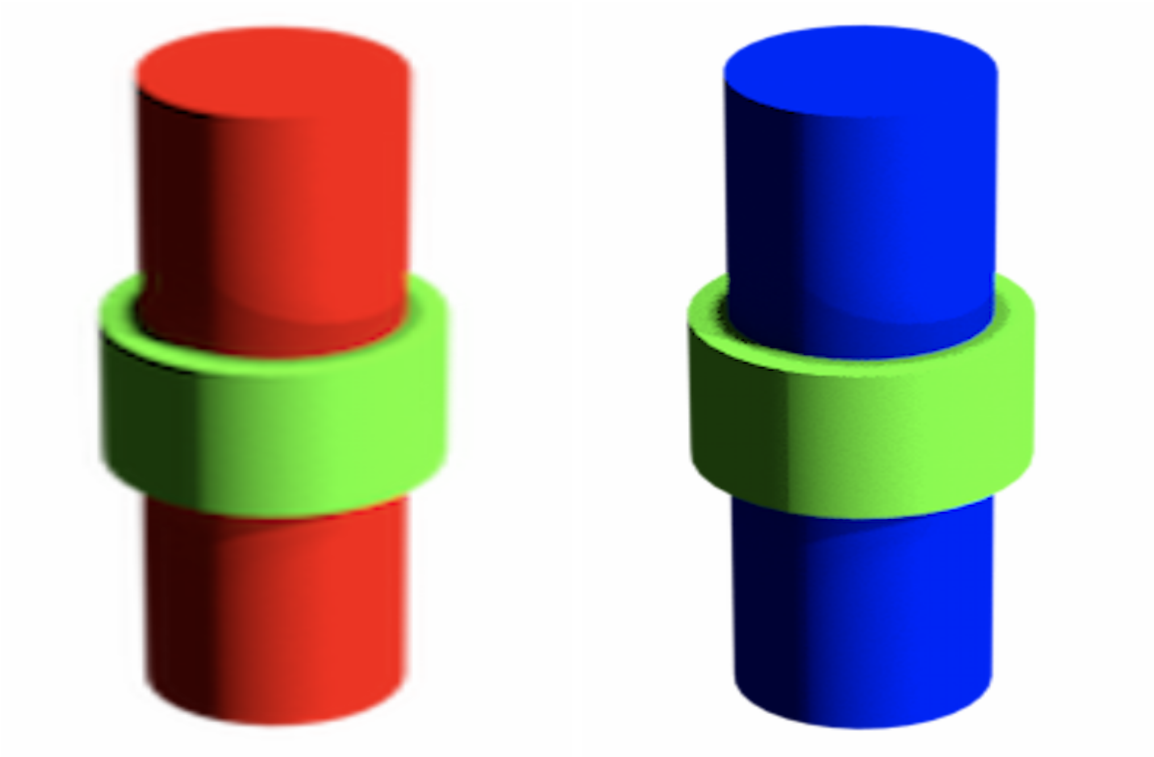


Figure 2.4: *Mesh Short Channel Short Terminal NMOS Mesh. [7]*



(a) Short Channel Short terminal NMOS **(b)** Short Channel Short terminal PMOS

Figure 2.5: Shortest Device Channel:180nm, Source/Drain: 500nm

2.2.2 Short Channel Short Terminal PMOS

Similar to how an NMOS was explained in the earlier section, this section explains a PMOS. To make things easier, we just explain the differences in comparison to the Short Channel Short Terminal NMOS with respect to the various subsections described above. The fundamental difference between the PMOS and the NMOS is the direction of flow of the charge carriers. Conventionally, the on current in an NMOS, flows from the drain to the source whereas in case of a PMOS, the on current will flow in the opposite direction from the source to the drain. The channel still remains intrinsically doped. The exact working of a PMOS Transistor is exactly the opposite to that of an NMOS device. The SCST PMOS is similar in construction to an SCST NMOS, except for the carrier doping concentration. For an NMOS, electrons are the majority charge carriers whereas for the PMOS holes are the majority charge carriers. So, we use the Boron as a dopant material in the PMOS although Phosphorous is used in the NMOS. The dimensions for this transistor are same as that of a corresponding NMOS device.

```
(sdedr:define-constant-profile "DrainDefinition" "BoronActiveConcentration" 1e+20)
(sdedr:define-constant-profile-region "DrainPlacement" "DrainDefinition" "drain")
(sdedr:define-constant-profile "SourceDefinition" "BoronActiveConcentration" 1e+20)
(sdedr:define-constant-profile-region "SourcePlacement" "SourceDefinition" "source")
```

Listing 2.4: Doping Statements for a PMOS

The code frame 2.4 shown above indicates that the only changes that need to be done while making a PMOS. We change carrier concentration from Phosphorous to Boron. The device is shown in the figure below inside the tool framework as well. Figure 2.5b shows the geometry of the PMOS device that was simulated with the red color representing an N type region.

2.2.3 Long Channel Long Terminal NMOS and PMOS

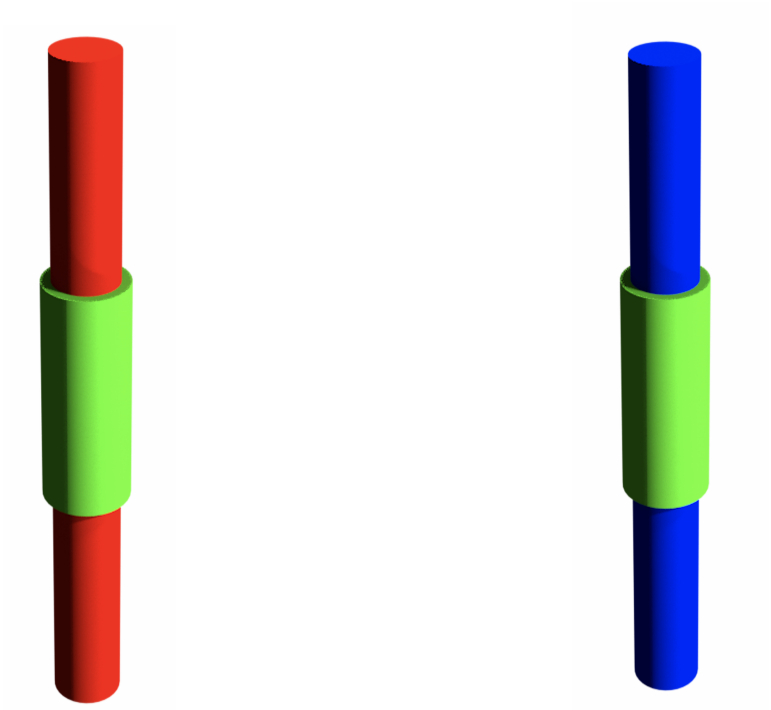
This section talks about the Long Channel Long Terminal device (Device Today). The structure, doping and the meshing properties are explained for both the N-type and the P-type device. The 3 main regions of the transistor are longer in length as compared to the shorter device. The SCST device has a channel that spans 180nm in length, whereas the source and drain terminals are 500nm long. In the Long Channel Long Terminal device, the channel length is 5 microns while the source and the drain terminals are also 5um. The radius of both the types of devices are around 50nm. The Long Channel Long Terminal transistor is again a perfectly gate aligned device with the gate oxide stacked directly on top of the channel region. The perfectly stacked device helps us to analyze the capacitance assuming a coaxial geometry. Analyzing a coaxial geometry makes the complex capacitance calculations much easier and save us the tedious process of going through AC simulations on the device simulator which also take a lot of time. Doping concentrations are the same as the SCST device with the channel remaining intrinsically doped as well and the source/drain with a 10^{20}cm^{-3}. The longer channel is one of the important factors in deciding the drive current of the device. The Phosphorus keyword is used in the doping statements for the NMOS device and the Boron for the PMOS device.

```
(sdegeo:create-cylinder (position 0 0 2.5) (position 0 0 -2.5)  0.05 "Silicon" "channel")
(sdegeo:create-cylinder (position 0 0 2.5) (position 0 0 7.5)  0.05 "Silicon" "drain")
(sdegeo:create-cylinder (position 0 0 -2.5) (position 0 0 -7.5)  0.05 "Silicon" "source")
(sdegeo:set-default-boolean "BAB")
(sdegeo:create-cylinder (position 0 0 -2.5) (position 0 0 2.5)  0.055 "SiO2" "oxide")
```

Listing 2.5: Geometry Statements indicating a longer channel device

The code frame 2.5 shown above indicates that the channel extends from -2.5um to 2.5um in the Z direction with the tube symmetric around the origin. The Old replaces New overlap behaviour is used for the oxide (SiO_2) deposition. The electrodes: gate, drain and the source are contacted at the different faces of the cylinder. The meshing strategies remain the same for all the three devices. The meshes have been designed in a way that

optimizes the run-time of the simulation and also the accuracy of the results. The following figures show the NMOS and the PMOS.



(a) Long Channel Long terminal NMOS **(b)** Long Channel Long terminal PMOS

Figure 2.6: Longest Device Channel: 5um, Source/Drain: 5um

2.2.4 Short Channel Long Terminal NMOS and PMOS

This is the last device that has been explored as a part of this project. The Short Channel Long Terminal Transistor is an intermediate device between the Short Channel Short Terminal and the Long Channel Long Terminal device. The source and the drain are 5um long as in Long Channel Long Terminal Device while the channel is 180nm which is same as the Short Channel Short Terminal device. The radius of both the PMOS and the NMOS transistors are 50nm. The doping is same as the previous two types of devices. A Phosphorous concentration of 10^{20}cm^{-3} for the NMOS and a Boron concentration 10^{20}cm^{-3} for the PMOS. The device is again an aligned device where the oxide is perfectly aligned with the channel region. The following code frame explains how the dimensions and the placement are different from the other devices.

```
(sdegeo:create-cylinder (position 0 0 0.09) (position 0 0 -0.09) 0.05 "Silicon" "channel")
(sdegeo:create-cylinder (position 0 0 0.09) (position 0 0 5.09)  0.05 "Silicon" "drain")
(sdegeo:create-cylinder (position 0 0 -0.09) (position 0 0 -5.09) 0.05 "Silicon" "source")
(sdegeo:set-default-boolean "BAB")
(sdegeo:create-cylinder (position 0 0 -0.09) (position 0 0 0.09) 0.055 "SiO2" "oxide")
```

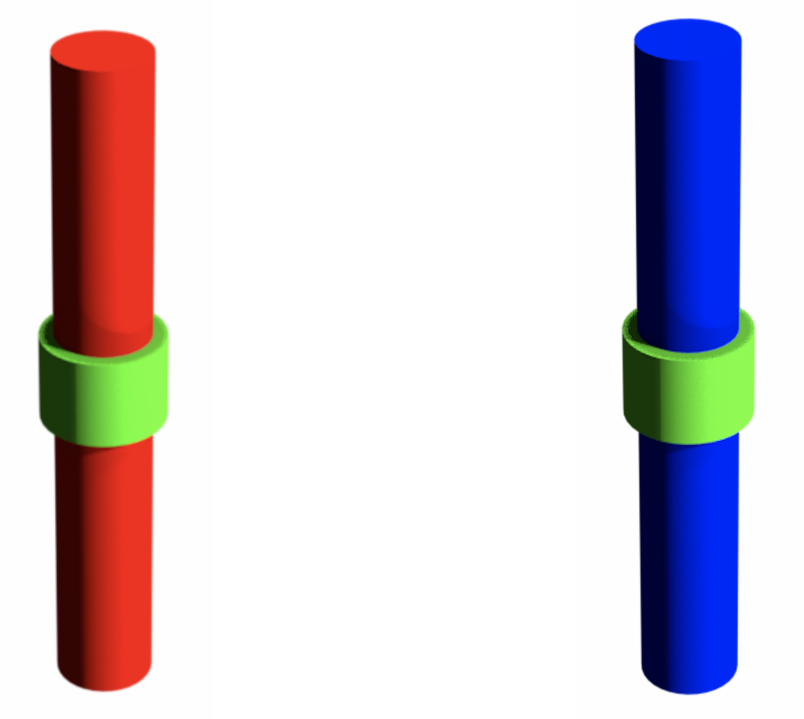
Listing 2.6: Shorter Channel and a Longer Geometry device

This device inherits some properties from both the devices discussed above because of its long terminals and the short channel.

```
(sdedr:define-constant-profile "DrainDefinition" "BoronActiveConcentration" 1e+20)
(sdedr:define-constant-profile-region "DrainPlacement" "DrainDefinition" "drain")
(sdedr:define-constant-profile "SourceDefinition" "BoronActiveConcentration" 1e+20)
(sdedr:define-constant-profile-region "SourcePlacement" "SourceDefinition" "source")
```

Listing 2.7: Doping for a Short Channel Long Terminal PMOS device

The listing 2.7 shows us how the doping is done for the Short Channel Long Terminal PMOS. Figures 2.7a and 2.7b describe the structure of the figures.



(a) Short Channel Long terminal NMOS **(b)** Short Channel Long terminal PMOS

Figure 2.7: Intermediate Device Channel: 180nm, Source/Drain: 500nm

2.3 Device Simulation and Sentaurus Device:

Understanding of the device simulator is really important to assimilate how the physics is solved inside the tool. The tool takes the mesh file from the previous step as input and solves the device, sweeping over the voltages at different terminals, leading to an output file that can be viewed in Sentaurus Visual. This section explains bit-by-bit the script that is used to simulate an NMOS device and obtain simple Id-Vg current characteristics. For a PMOS device, the corresponding electron continuity equations are replaced with the hole continuity equations.

```
File {
  Grid = "ShortChannel_ShortTerminal_NMOS_msh.tdr"
  Plot = "ShortChannel_ShortTerminal_NMOS.dat"
  Current = "ShortChannel_ShortTerminal_NMOS.plt"
  Output = "ShortChannel_ShortTerminal_NMOS.log"
}
Electrode {
  { Name="gate" Voltage = 0 WorkFunction = 4 }
  { Name="source_c0" Voltage = 0}
  { Name="drain_c0" Voltage = 0 }
}
Physics {
  Mobility (
    Enormal(IALMob)
    HighFieldSaturation
  )
  EffectiveIntrinsicDensity( OldSlotboom )
  Recombination( SRH(DopingDep) )
  eQuantumPotential
}
```

Listing 2.8: File, Electrode and Physics Section

The code shown in listing 2.8 consists of the file, electrode and the physics section. In the file section, various input and output files are defined to be used in the simulation. Plot files will have numerical values pertaining to the simulation specified. Log files are effective in helping to resolve errors and debug the issues encountered during simulations. The

Electrode section is responsible for defining the electrodes corresponding to the terminals and then the respective boundary conditions at these terminals. The Workfunction of the gate stack can be manipulated here to obtain a shift in the threshold voltage of the device. The various models used in the physics section are explained below:

- **Mobility Models**: The mobility models define how the mobilities of carrier work at the interface and inside the channel. The intrinsic and the accumulation Layer mobility models are specified for the simulation run.
- **Bandgap Modelling**: For semiconductor devices, the most fundamental property is the band structure. The OldSlotboom model is selected for the band energy structure.
- **Recombination Models**: SRH models are used which lead to recombination through deep defect levels in the gap.
- **Quantum Potential**: Quantum Potential has also been considered while solving the device. We use electron Quantum Potential while solvnig for an NMOS and Hole Quantum Potential while solving for a p-type device.

```
Plot{
  eDensity hDensity eCurrent hCurrent
  TotalCurrent/Vector eCurrent/Vector hCurrent/Vector
  eMobility hMobility eVelocity hVelocity
  eEnormal hEnormal
  ElectricField/Vector Potential SpaceCharge
  eQuasiFermi hQuasiFermi
  Potential Doping SpaceCharge
  SRH Auger AvalancheGeneration
  DonorConcentration AcceptorConcentration Doping
  eGradQuasiFermi/Vector hGradQuasiFermi/Vector
  eEparallel hEparalllel BandGap BandGapNarrowing
  Affinity ConductionBand ValenceBand
  eQuantumPotential hQuantumPotential
    }
Math {
  -CheckUndefinedModels
```

```
  Number_Of_Threads=4
  Extrapolate
  Derivatives
  RelErrControl
  Digits=5
  ErRef(electron)=1.e10
  ErRef(hole)=1.e10
  Notdamped=50
  Iterations=50
  Directcurrent
  Method=ParDiSo
  Parallel= 2
  NaturalBoxMethod
     }
```

Listing 2.9: Plot and the Mathematical Models

The frame in the listing 2.9 delineates the various vector and scalar quantities to be plotted once the device simulations are done. It also defines the various mathematical models to be used while solving the numerical equations. For Example: The error reference for an electron and hole equation is 10^{10}. Maximum iterations are set to 50 and so forth.

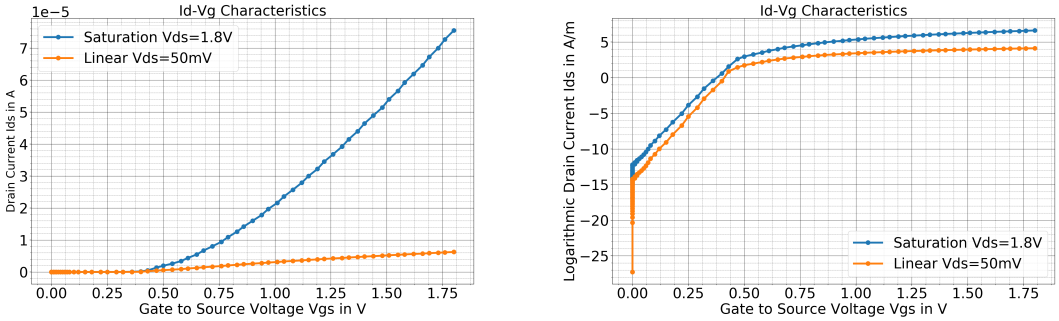
```
Solve {
  Coupled ( Iterations= 150){ Poisson eQuantumPotential }
  Coupled { Poisson eQuantumPotential Electron Hole }

  Quasistationary(
    InitialStep= 1e-3 Increment= 1.2
    MinStep= 1e-12 MaxStep= 0.95
    Goal { Name= "drain_c0" Voltage= +2.5 }
  ){ Coupled { Poisson eQuantumPotential Electron Hole } }

  Quasistationary(
    InitialStep= 1e-3 Increment= 1.2
    MinStep= 1e-12 MaxStep= 0.02
    Goal { Name= "gate" Voltage= +2.5 }
    DoZero
  ){ Coupled { Poisson eQuantumPotential Electron Hole } }
}
```

Listing 2.10: Solve Section for device simulation

The Solved section is one of the most important parts of a device simulator code. The first step specifies that the initial solution is of the nonlinear **Poisson** equation and the **eQuantumPotential** (hQuantumPotential in case of a PMOS) equation with the initial biases at the electrodes applied. The second step introduces the Electron and the Hole continuity equation. All the equations are fully coupled to each other utilizing the solution from the previous step as the initial solution for the next step in the Newton method. The Quasi-stationary statement specifies that quasi-static or steady state equilibrium solutions are to be obtained. A set of Goals for one or more electrodes is defined in parentheses. In this case, a sequence of solutions is obtained for increasing drain bias up to and including the goal of 2.5 V. Then, the gate is ramped up from 0 to 2.5V to sweep the gate bias to obtain the current. A fully coupled method for the self-consistent solution of the Poisson, electron continuity, hole continuity and electron (hole) quantumpotential equations is specified in braces. Again each bias step is solved by taking the solution from the previous step as its initial guess. There is also the freedom to control the Initial Step, Maximum and the Minimum steps to aid the tool in convergence.

2.4 Results of Device Simulation:

This section will focus on evaluation of all the device simulations. We first discuss the basic results of the device simulation for all three N Channel MOSFETs. We evaluate two modes of operation: Saturation and Linear mode of operation. Saturation Mode corresponds to a Supply Voltage (Drain to Source Voltage: V_{ds}) of 1.8V. This mode of operation leads to the maximum on current through the device channel consequently leading to minimum device resistance. The linear mode corresponds to a region of operation with a Supply Voltage (Drain to Source Voltage: V_{ds}) of 50mV.



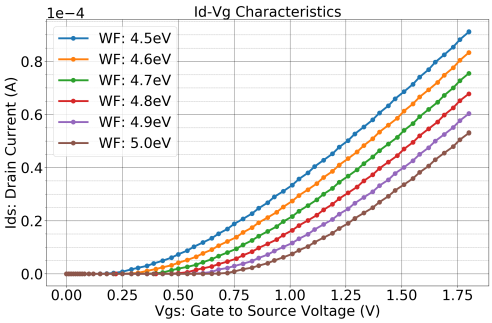
(a) Linear Characteristics

(b) Logarithmic Characteristics

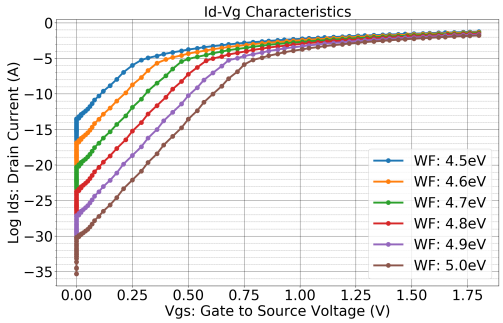
Figure 2.8: Drain Current vs Gate Voltage for Short Channel Short Terminal Device

As observed from 2.8a, we can see that the threshold voltage of the device is around 0.47V. The ON-Current for the device in saturation mode is around 70 μA, while that in linear mode is around 7 μA. The workfunction of the gate electrode has been sweeped from 4.5eV to 5eV. This sweep results in a sweep of the gate threshold voltage from around 0.25V to 0.75V. To select a device for further analysis, we choose a device which has an ON-Current to OFF-Current ratio of about 10^5. We benchmark our devices against standard 180nm CMOS devices. They used a V_{ds} of around 1.8V. Due to this, our gate voltages V_{gs} are sweeped from 0 to 1.8V with V_{ds} of 1.8V.

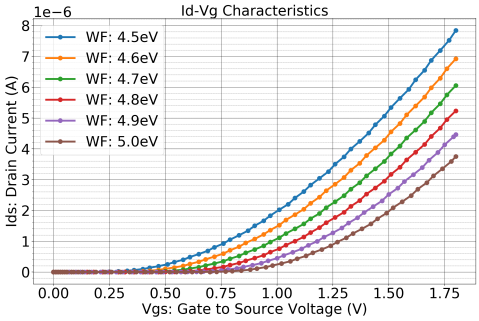
Figure 2.9 plots the resultant I_d-V_{gs} obtained after sweeping the workfunction of the gate electrode. This plots the curves at different Threshold Voltages V_t. The Threshold volt-



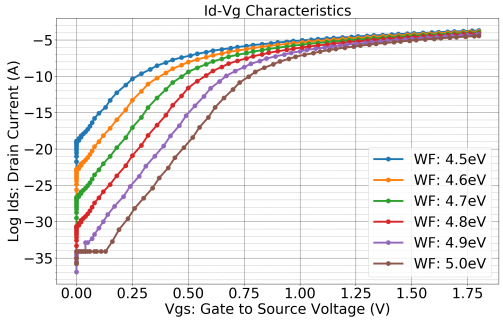
(a) Workfunction Sweeps SCST



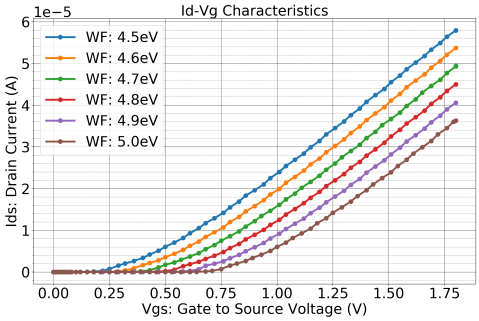
(b) Logarithmic Workfunction Sweeps SCST



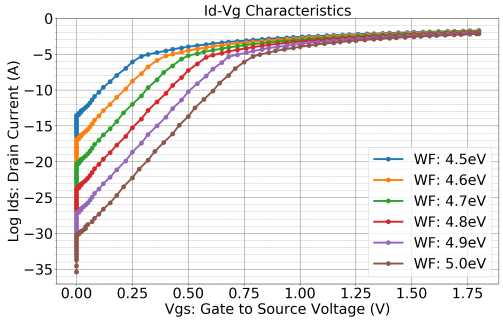
(c) Workfunction Sweeps LCLT



(d) Logarithmic Workfunction Sweeps LCLT



(e) Workfunction Sweeps SCLT

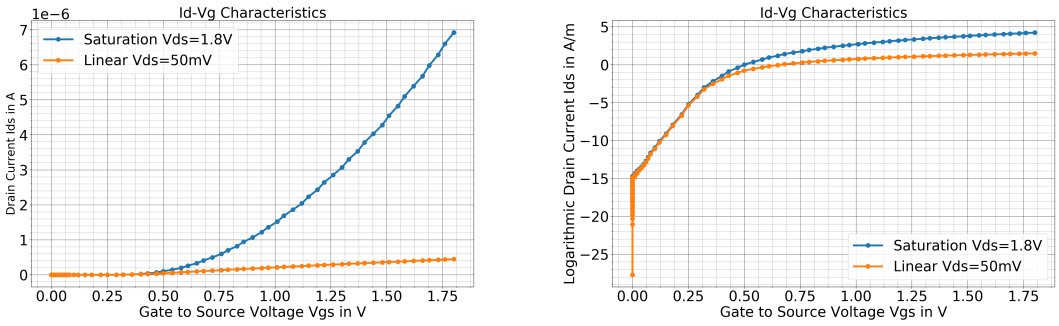


(f) Logarithmic Workfunction Sweeps SCLT

Figure 2.9: WorkFunction Sweeps to decide threshold voltage of the device.

age of the device is dependent on the Metal-Gate WorkFunction of the electrode. Higher the Workfunction, higher the threshold voltage, lesser is the on current and hence consequently more is the off current of the device. Since the Long Channel Long Terminal device has a longer channel and the terminals compared to a short channel short terminal end of the roadmap device, we observe that due to this channel resistance, the on current of this device is considerably smaller than the Short Channel Short Terminal device. Figure 2.10

plots the logarithmic and the linear plots for Drain Current to Gate Voltage Characteristics to show the drop in the ON Current for this larger device. Again this par-

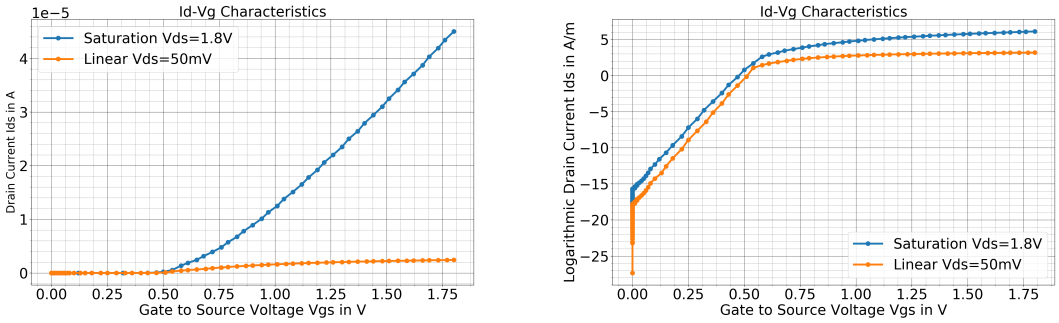


(a) Linear Characteristics **(b)** Logarithmic Characteristics

Figure 2.10: Lower ON current for a Long Channel Long Terminal Device

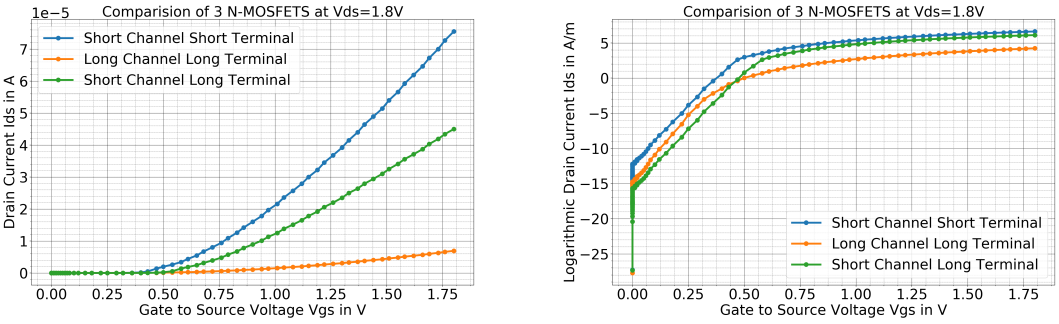
ticular device V_t has been selected using the ON-Current/OFF-Current Ratio as a criteria. We choose a device which has this criteria satisfied with a value of 10^5. Figures 2.9c and 2.9d are plots for various I_d-V_{gs} curves for varying V_t. A lower on current is because of the fact that the device will have a larger gate capacitance because of the sheer size of the gate contacted over the channel region. This lower on current coupled with higher capacitance seriously affects the device's capability to drive a CMOS based circuit which is explored in the later sections. The Short Channel Long Terminal Transistor is intermediate between the 2 extremes (Short Channel Short Terminal and Long Channel Long Terminal). It inherits some properties of both of the devices. Because of the longer source/drain terminals, it has some resistance in the current path, thereby leading to a decrease in the ON-Current of the device. On the other hand, the length of the channel for an SCLT device is same as the SCST device, so it also has current drive closer to that of the End of the Road Map device. Figures 2.11a and 2.11b demonstrate this from the current curves. The NMOSes as discussed in the device above show that due a Gate All Around type of geometry, it has a much tighter control over the electrostatics and hence leads to an improved ON-Current as compared to a standalone 180nm N-Channel MOSFET. Figures 2.12 and 2.13 show how

the three devices stand with repsect to each other.



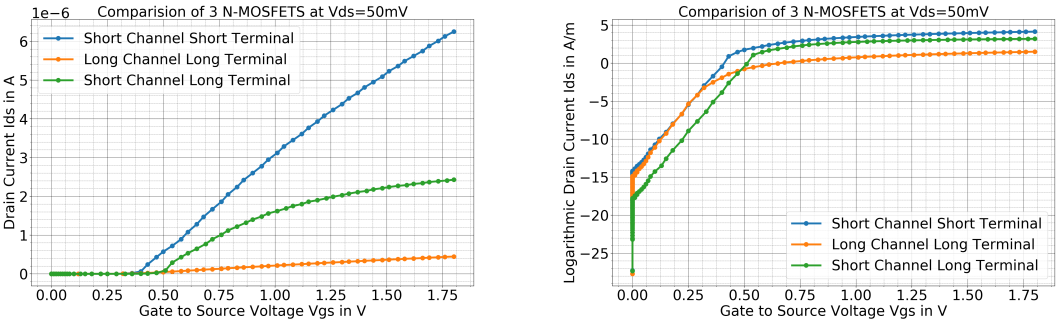
(a) Linear Characteristics **(b)** Logarithmic Characteristics

Figure 2.11: Short Channel Long Terminal Device has lower current than an ideal device.



(a) Linear Characteristics **(b)** Logarithmic Characteristics

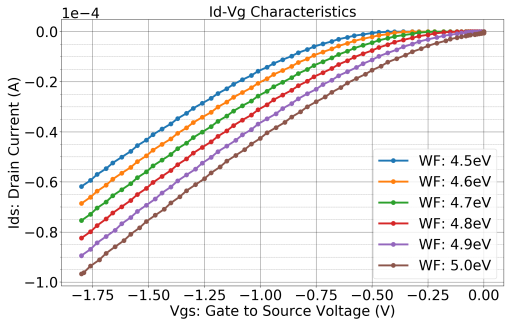
Figure 2.12: Saturation Region Comparisons of all 3 NMOSes for clarity



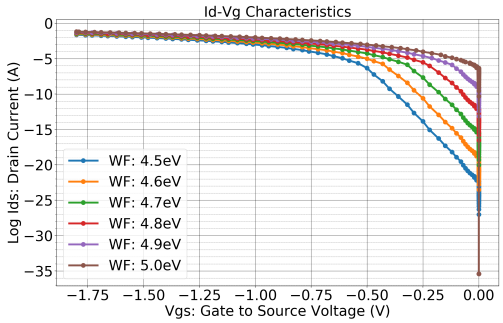
(a) Linear Characteristics **(b)** Logarithmic Characteristics

Figure 2.13: Linear Region ON-Current for all 3 devices.

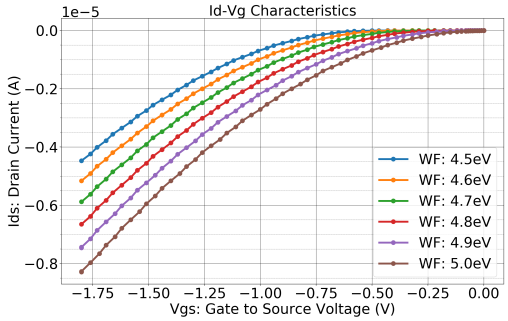
The P-Channel MOSFETS also had similar observations. We start by sweeping the PMOS transistor for all 3 geometries for varying workfunctions to eventually obtain a shift



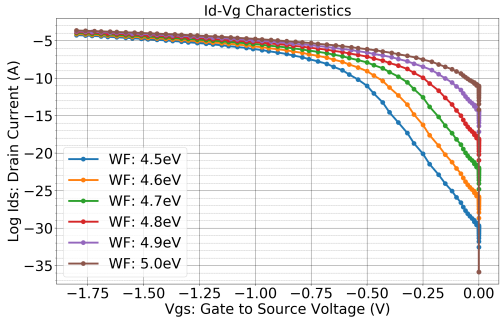
(a) Workfunction Sweeps SCST



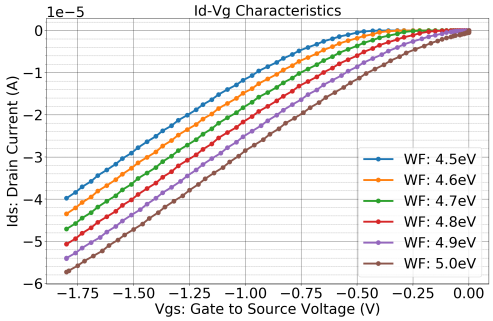
(b) Logarithmic Workfunction Sweeps SCST



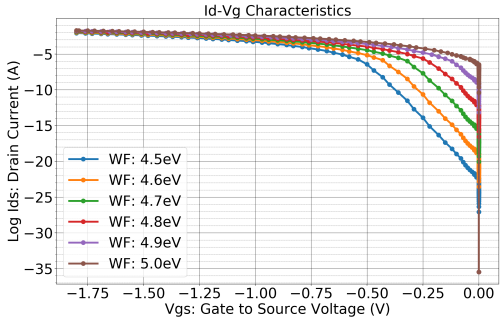
(c) Workfunction Sweeps LCLT



(d) Logarithmic Workfunction Sweeps LCLT



(e) Workfunction Sweeps SCLT

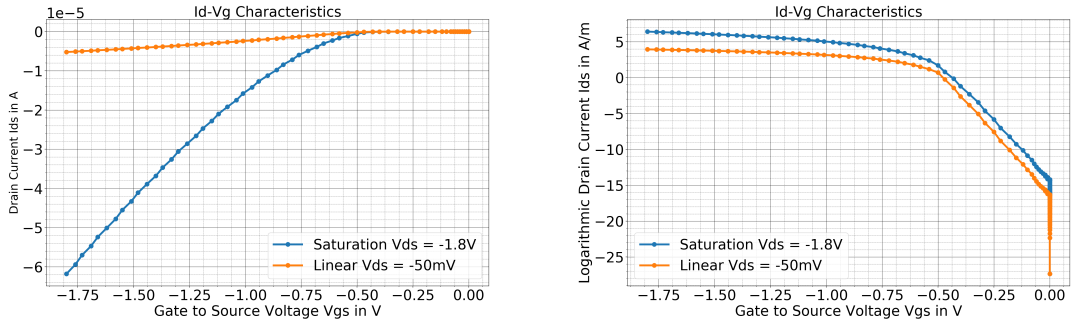


(f) Logarithmic Workfunction Sweeps SCLT

Figure 2.14: WorkFunction Sweeps to decide threshold voltage of the device.

in the threshold voltage V_t. Once we have that, we have the same criteria of the ON-Current to OFF-Current ratio (value of about 10^5) to select a corresponding PMOS. We also have an additional criteria here to select a PMOS device to match the corresponding selected N Channel MOSFET. The ON-Current of NMOS should be around 2-3 times that of PMOS. A larger NMOS ON-Current would lead to skewed operation of the devices while analyzing the implications of a standard CMOS logic style, where it would take longer for

the circuit to be pulled to a logic high level. Figure 2.14 evaluates the performance of all the PMOS devices at varying V_t to aid in the final selection of the PMOS device. The P-Channel MOSFETs have holes as the majority charge carriers as compared to electrons in the N-Channel MOSFET. The presence of hole just indicates that an electron is absent from a particular region. This will imply that the operation of the PMOS and will be exactly opposite to that of an NMOS. So, the supply voltages and the input voltages will be reversed as comparision to an NMOS. For an NMOS the V_{ds} is at 1.8V or 50mV while for a PMOS, the V_{ds} is at -1.8V for saturation region or at -50mV for the linear region of operation. Consequently, the current in the PMOS also flows in the opposite direction to that of an NMOS device. The current in the reverse direction is shown by the reversal in the mathematical sign of the current.

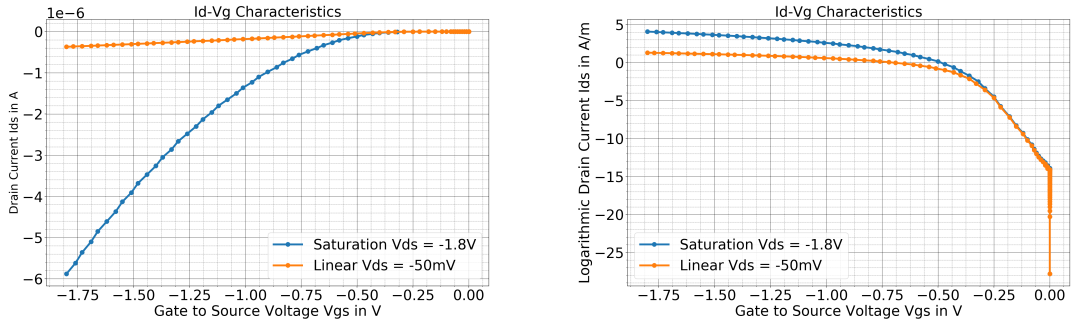


(a) Linear Characteristics **(b)** Logarithmic Characteristics

Figure 2.15: Short Channel Short Terminal PMOS.

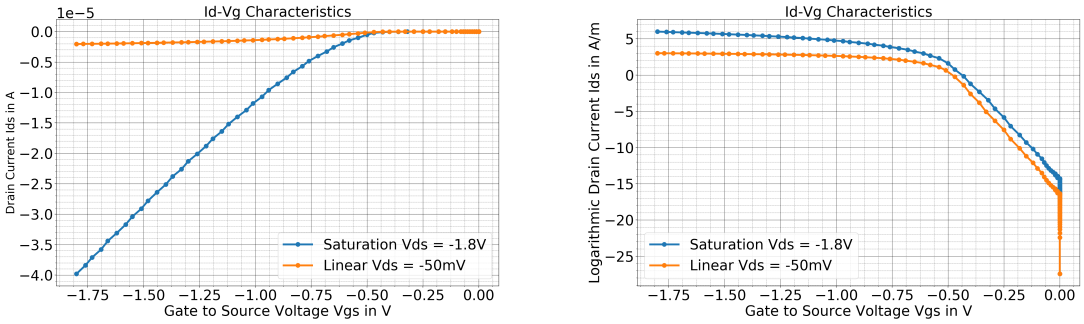
As shown in 2.15, the Short Channel Short Terminal PMOS has been simulated at a gate workfunction of about 4.5eV. The logarithmic current has been normalized by the width of the device. Similar observations have been made for the Long Channel Long Terminal PMOS as were for the Long Channel Long Terminal NMOS. The drive current reduces significantly from the Short Channel Short Terminal device. This is plotted in Figure 2.16.

This reduction in the ON-Current is attributed to the increase in the length of the channel from 180nm to 5um. The Largest PMOS device has been evaluated at a Metal Gate



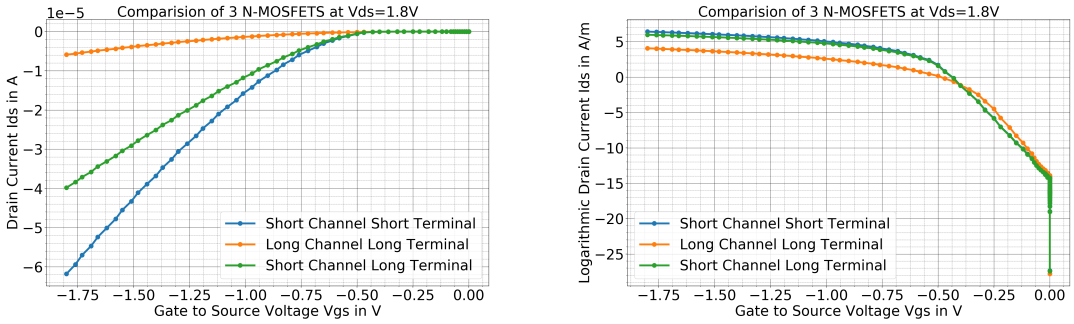
(a) Linear Characteristics **(b)** Logarithmic Characteristics

Figure 2.16: Long Channel Long Terminal PMOS.



(a) Linear Characteristics **(b)** Logarithmic Characteristics

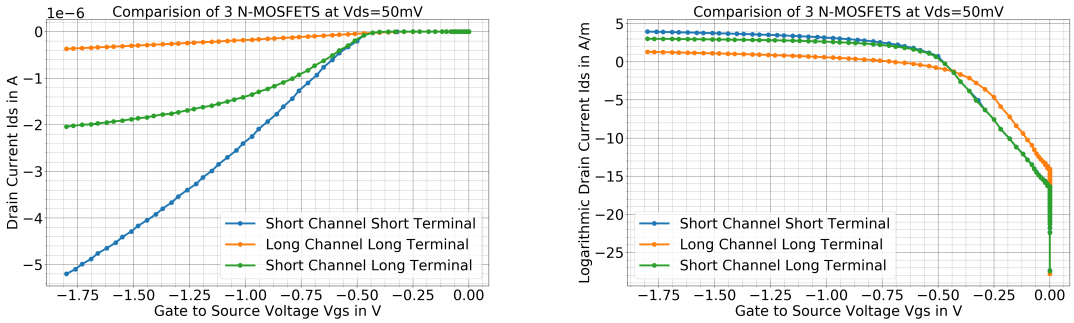
Figure 2.17: Short Channel Long Terminal PMOS has lesser current as compared to a SCST PMOS but more than that of the LCLT PMOS.



(a) Linear Characteristics **(b)** Logarithmic Characteristics

Figure 2.18: Saturation Region Comparisons of all 3 PMOSes for clarity

Workfunction of around 4.7eV. For a PMOS, the intermediate device has been shown to follow the similar trend to an intermediate NMOS in terms of an ON-Current. Figure 2.17 has been used to show how a Short Channel Long Terminal PMOS behaves. To draw com-



(a) Linear Characteristics **(b)** Logarithmic Characteristics

Figure 2.19: Linear Region Comparisons

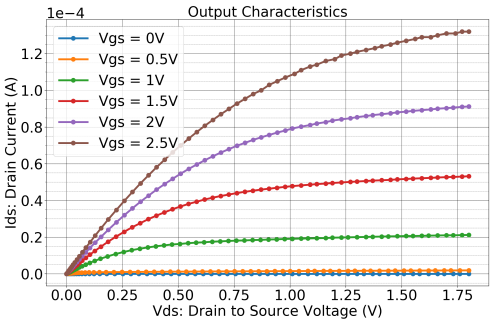
parisons of three devices with respect to each other, we use Figure 2.18a which compares the devices in Saturation mode of operation (V_{ds} = 1.8V) and Figure 2.19a which uses linear mode (V_{ds} = 50mV) for comparison.

For a better analysis in terms of the behaviour of the device, we have also plotted the Output Characteristics of the device. The Output characteristics of a transistor is basically a plot with Drain Source Current I_{ds} on the Y axis with the Drain Source Voltage V_{ds} on the X axis, with varying values of Gate Source Voltage V_{gs}. We sweep the V_{ds} from 0 to 1.8V with different V_{gs} values of 0V, 0.5V, 1V, 1.5V, 2V, 2.5V for an NMOS, whereas V_{ds} is sweeped from -1.8 to 0V with different V_{gs} values of 0V, -0.5V, -1V, -1.5V, -2V, -2.5V for an PMOS. The family of these curves for the 3 NMOSes and the 3 PMOSes has been shown in figure.

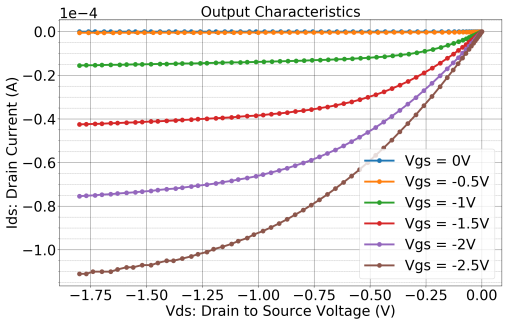
The following table will summarize all the important parameters of all the 6 devices.

Table 2.1: Summary of Important Device Parameters

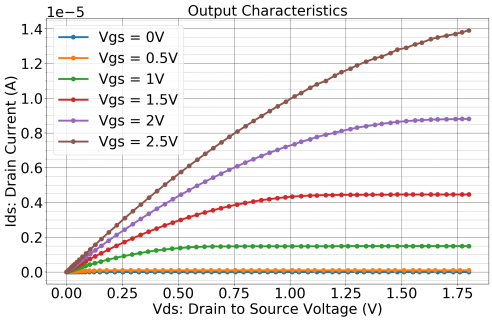
Device	Work Function(eV)	$I_{ON}(\mu A)$	$I_{OFF}(\mu A)$	$V_t(V)$	I_{ON}/I_{OFF}
SCST NMOS	4.7	7.54×10^{-5}	4.35×10^{-13}	0.47	1.73×10^{8}
LCLT NMOS	4.6	6.92×10^{-6}	3.49×10^{-14}	0.51	1.98×10^{8}
SCLT NMOS	4.8	4.50×10^{-5}	1.35×10^{-14}	0.52	3.33×10^{9}
SCST PMOS	4.5	-6.18×10^{-5}	-5.91×10^{-14}	-0.55	1.05×10^{9}
LCLT PMOS	4.7	-5.88×10^{-6}	-7.91×10^{-14}	-0.5	7.43×10^{7}
SCLT PMOS	4.5	-3.97×10^{-5}	-5.58×10^{-14}	-0.5	7.11×10^{8}



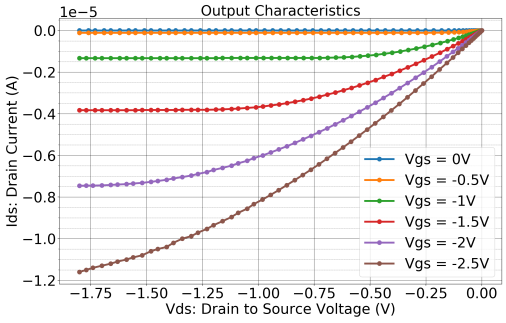
(a) Output Characteristics for NMOS SCST



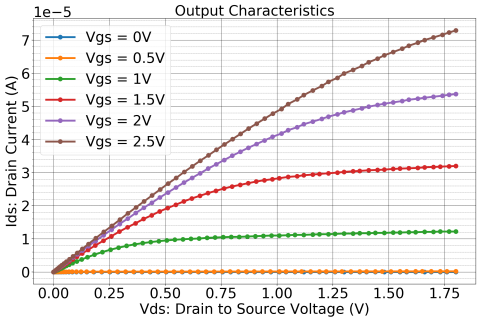
(b) Output Characteristics for PMOS SCST



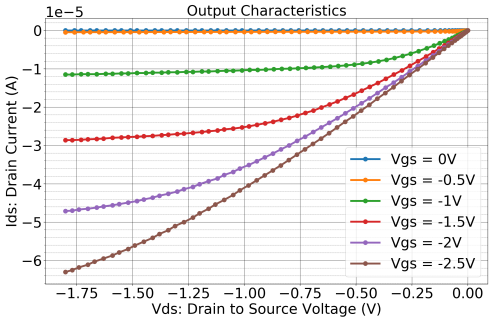
(c) Output Characteristics for NMOS LCLT



(d) Output Characteristics for PMOS LCLT



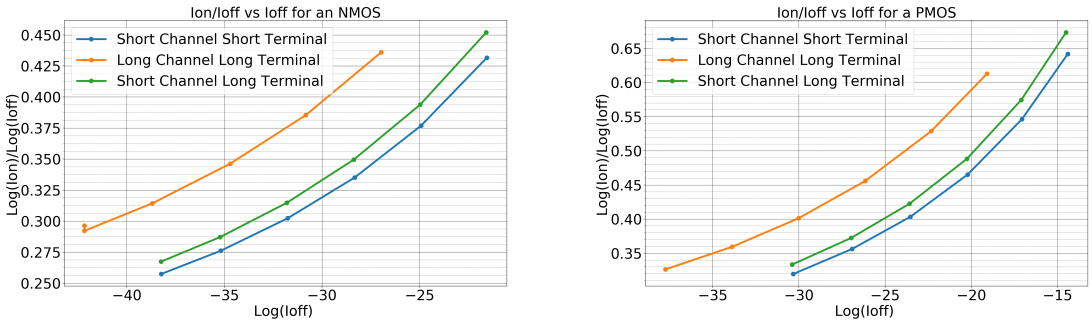
(e) Output Characteristics for NMOS SCLT



(f) Output Characteristics for PMOS SCLT

Figure 2.20: Family of Curves for all 6 devices to represent Output Characteristics.

The following curves in figure 2.21 plot the Log(I_{ON})/Log(I_{OFF}) vs Log(I_{OFF}). As we move towards the left along any curve, the Log(I_{OFF}) becomes negative, implying that off current reduces thereby consequently inferring a decrease in the Threshold Voltage of the device.



(a) NMOS Devices **(b)** PMOS Devices

Figure 2.21: Curves of $Log(I_{ON})/Log(I_{OFF})$ vs $Log(I_{OFF})$

CHAPTER 3

IMPLICATIONS OF LARGE AREA ELECTRONICS OB DIGITAL CIRCUITS

We established a thorough understanding of the devices in the previous section. This section, we move onto discussing some work in circuits. We discuss how these large area Gate All Around devices affect the performance of some basic digital circuits. We investigate circuits like CMOS Inverter, CMOS Inverter-Fanout 1, CMOS Inverter-Fanout 4, CMOS NAND, CMOS NOR, RING OSCILLATORS and a Full Adder. We analyze all these circuits with respect to all our three devices (Short Channel Short Terminal, Long Channel Long Terminal, Short Channel Long Terminal). We also analyze and explore the parasitics between the two devices and circuits as well. To analyze the circuits and their performance, we need to define a capacitance model associated with the device. Usually simulating a capacitance by performing an AC Simulation on the device simulator like Sentaurus TCAD has a much larger runtime than the device simulations performed for a regular DC sweep. We therefore use a model for the device capacitance which we describe in the next section. Once, the device capacitance has been set, the different circuits are analyzed for a transient response to verify their functional correctness and understand their performance for all the three devices. Switching Speeds and frequencies as a function of the interconnect length between devices have been explored in much detail as a focus of this thesis. We benchmark our technology against a 180nm Predictive Technology Model CMOS Technology. Spectre Simulator by Cadence has been used for the extensive circuit analysis performed. [11]

3.1 Device Capacitance

This section focuses on establishing a model for the device capacitance used for analyzing the circuits. The first approach to obtaining a device capacitance value which is complementary with the table model Verilog-A being implemented for the I_d-V_{gs} is to get a similar table model lookup for the Capacitance (C-V_{gs} and C-V_{ds}) as a function of the gate voltage. But the AC Simulation runtime coupled with the requirement of multiple V_{ds}-V_{gs} isolines for capacitance value can make it a difficult solution. To bypass this problem, we take advantage of the fact that our devices are a class of the large area flexible electronics. Being cylindrical in geometry makes it much easier to model capacitance. We model the capacitance for our nanowires by comparing it to a capacitance of a simple cylindrical structure. The figure 3.1 shows the geometry of device used for modelling capacitance values.

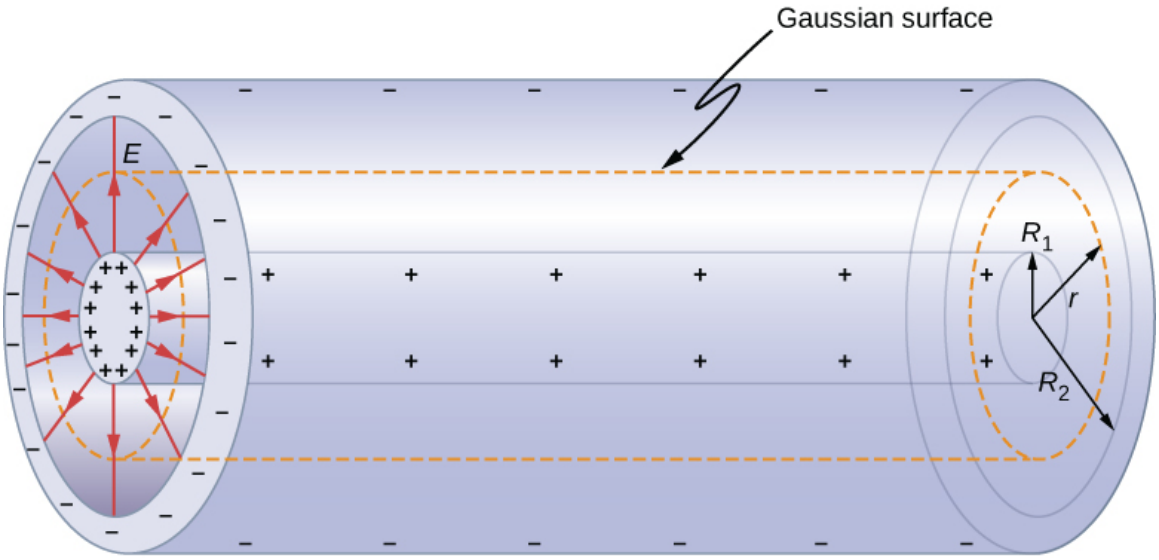


Figure 3.1: Capacitance Model for the Nanowire

The capacitance model can be estimated by the following equation:

$$\frac{C}{L} = \frac{2\pi\epsilon_r}{\ln\frac{b}{a}} \tag{3.1}$$

where C/L stands for Capacitance per unit Length, ϵ_r indicates the dielectric constant of the oxide, b signifies the outer radius and a signifies the inner radius of the device.
The devices are analyzed on the basis of the fact that they are perfectly aligned devices. If that wasn't the case, then the device capacitance would be dominated by the overlap capacitance rather than the junction capacitance. The dimensional aspects of the three devices described in the previous section are summarized below.

- **Short Channel Short Terminal (SCST):** Channel length is 180nm. The gate is a perfectly aligned gate. So, the oxide and the channel are exactly on top of each other with the oxide **not** overlapping either the source or the drain. Hence, the length of the oxide is 180nm.

- **Long Channel Long Terminal (LCLT):** Channel Length is 5μm for the longest device. Since, it is a self aligned device, the oxide is 5μm as well.

- **Short Channel Long Terminal (SCLT):** This is the intermediate device between the longest and the shortest devices. It has larger terminals like the LCLT device while a short channel like the SCST device. Oxide length is therefore 180nm.

Device capacitance is calculated by plugging in the values in equation 3.1. We have the following results for a SCST and a SCLT device: C = 0.356fF whereas for the Long Channel device we get the value of C = 9.889fF. Establishing this as the cap values, we analyze the performance of various digital circuits with respect to the three devices.

3.2 CMOS Inverter

The CMOS Inverter is one of the most fundamental digital circuits. It is composed of one N-Channel Transistor and one P-Channel Transistor. The circuit diagram and the symbol of a basic Static CMOS Inverter is shown in the figure 3.2.

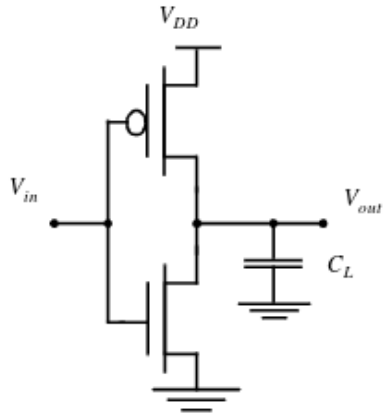


Figure 3.2: Inverter Schematic [12]

Table 3.1: Truth table of an Inverter

Input	Output
0	1
1	0

The working of a static CMOS Inverter can be easily understood by understanding the operation of a PMOS and an NMOS transistor as a switch. The Transistors will have three modes of operation viz. Cutoff, Linear and Saturation. These operating regions of the transistors are a function of the input voltage and the supply voltage of the transistor. The operating regions of the NMOS transistor are explained below. The operation of a PMOS is exactly opposite to that of an NMOS.

- **Cutoff Region:** The transistor is in cutoff when the V_{gs} ¡ V_t. In the cutoff region the transistor behaves like switch with infinite off resistance. The I_{ds} is equal to the I_{OFF} of the device.

$$I_{\text{ds}} \simeq 0 \tag{3.2}$$

- **Linear Region:** In the linear region of operation, the current through the transistor is proportional to the voltage applied. This region happens when V_{gs} ¿ V_t and V_{ds} ¡ V_{gs} - V_t. The current through the device is given by the following equation.

$$I_{ds} = \mu_n C_{OX} \frac{W}{L} [(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}] \tag{3.3}$$

- **Saturation Region:** In this region of operation, the transistor behaves as an almost ideal current source, since the current remains constant. A change in voltage doesn't translate to a change in the current through the transistor. Hence, the current is defined as follows:

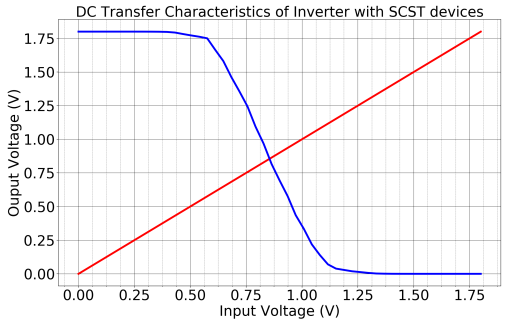
$$I_{ds} = \mu_n C_{OX} \frac{W}{L} (V_{gs} - V_t)^2 \tag{3.4}$$

The operation of inverter is based on the understanding of transistor as a switch. We can therefore interpret the working of the Inverter. When the Input Voltage V_{IN} is High (Logic 1), the NMOS transistor is ON. Since, the NMOS is on, the output node V_{OUT} has a direct path to the ground node, thereby pulling the output voltage to 0. On the other hand, if the input V_{IN} is Low (Logic 0), then the PMOS transistor is ON, establishing a direct path from the Supply Node V_{DD} to the output node V_{OUT}. For an ideal inverter, the PMOS and the NMOS transistors have no resistance, hence the output voltage swing is from GND to V_{DD}, resulting in a high Noise Margin. Also, the logic levels are not dependent on the ratio of the device sizes, thereby making it a ratioless circuit. The inverter is static because at any point of time during the steady state operation the output node is connected to either the V_{DD} or GND. No direct path exists between V_{DD} and GND during the steady state of operation (Inputs are constant). The input impedance of the gate of an NMOS or a PMOS is very high. Since, the input for an inverter is connected to the gates of the transistor, consequently the inverter has high input impedance leading to no DC current being drawn to the input. We discuss the DC Operation of an Inverter first and then move on to the Transient Behaviour of an Inverter

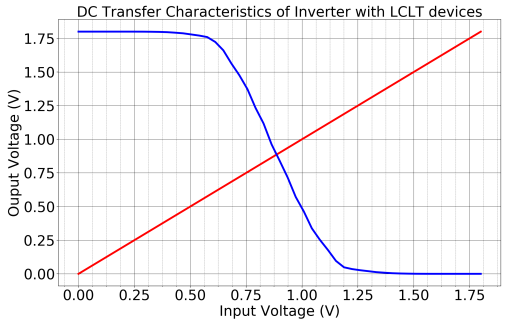
DC Transfer Characteristics of an Inverter

The DC Operation of an inverter specifies the operation of the circuit to a steady state stimulus. The DC Voltage is generally specified by plotting the Voltage Transfer Characteristics of the Inverter (VTC). It is a curve that plot the Output Voltage as a function of the Input Voltage. SCST, LCLT and SCLT devices have been used in our implementation of the inverter. Depending on the Input of the inverter, the transistors are in different modes whether cutoff, saturation or linear and the corresponding output of the inverter is determined. Since, we use a 180nm technology for benchmarking, to make it an apples-to-apples comparison we choose a supply voltage V_{DD} of 1.8V for our circuit experiments as well. We plot the VTC for our 3 devices and then finally the benchmark technology and contrast some of the DC parameters of the inverter for all the devices.

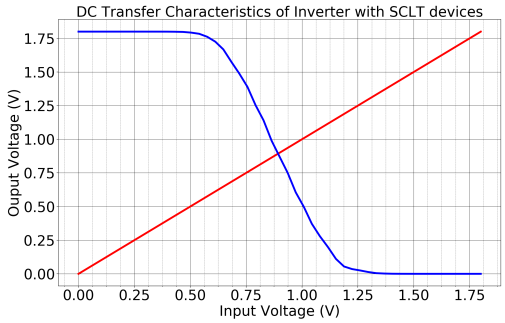
We now discuss various DC parameters like the Switching Threshold V_M and Noise Mar-



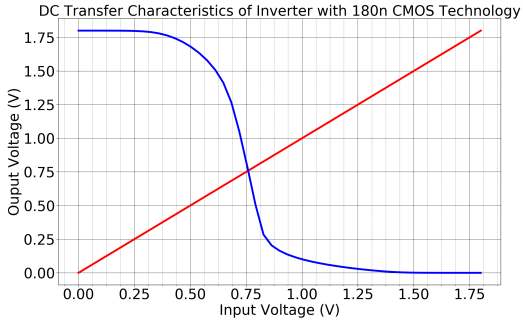
(a) Inverter VTC for the SCST Devices



(b) Inverter VTC for the LCLT Devices



(c) Inverter VTC for the SCLT Devices



(d) Inverter VTC for 180nm Benchmark Technology

Figure 3.3: Inverter Voltage Transfer Characteristics (VTC).

gins of the Inverter.

- *Switching Threshold of an Inverter*: The switching threshold of an inverter is defined as the point where the Inverter output switches states. It is also defined as the point where the two curves in the figure 3.3 intersect. As for the transistors, both the PMOS and the NMOS are always saturated in this region of operation of the inverter. So, one can obtain V_M analytically by equalling the saturation currents of the PMOS and the NMOS. When solved for the equation, it turns out that the switching theshold is usually dependent on the sizes of the PMOS and the NMOS. A wider PMOS (in our case of Nanowires, wider means multiple PMOS tubes in parallel) indicates that the device will take much longer to switch to Logic 0 as compared to Logic 1 and will shift the VTC curve to the right. On the other hand, more NMOS tubes in parallel indicate the ease of the Inverter to retain the Logic 0 state, thereby shifting the curve to the right. It is desirable therefore to get a V_M in the center region to minimize the possibility of getting a skewed inverter. The table below lists the measured value of the Inverter Threshold by simulating the above curves. Looking at the values of the

Table 3.2: Switching Thresholds of Inverter with different Devices

Device Technology	Switching Threshhold (V)
SCST	0.852
LCLT	0.885
SCLT	0.893
180nm PTM	0.759

table, we conclude that the ideal V_M should be around 0.9V for the inverter, but the 180nm PTM inverter is a skewed inverter with the NMOS stronger than the PMOS. Because of this, it's easier to switch the inverter from a logic 1 level to a logic 0 level.

- *Noise Margin of the Inverter*: Noise margin of an inverter is the ability of an inverter to reject noise and output the correct faithful value. Noise margin is calculated based on a number of parameters: V_{IH}. V_{IL}, V_{OH}, V_{OL}. We know from the DC Transfer curve that V_{OH} = V_{DD} and V_{OL} = GND for ideal inverters. Analytically, it is calculated that V_{IH} and V_{IL} are those points on the VTC curve where the slope is -1. V_{IH} and V_{IL} are those points on the inverter operation where the inverter starts to transition. V_{OL} and V_{OH} will be the output of the inverter corresponding to these voltages as input. They are the bounds of the transition region. The width of the transition regions are related to the Noise margins of the Inverter. Noise margins are defined by the equations as follows:

$$NM_{\mathrm{H}} = V_{\mathrm{OH}} - V_{\mathrm{IH}} \tag{3.5}$$

$$NM_{\mathrm{L}} = V_{\mathrm{IL}} - V_{\mathrm{OL}} \tag{3.6}$$

Higher the noise margin, more is the ability of the CMOS inverter to withstand noise without compromising the operation of the circuit. The slope of the curve is basically the gain of the inverter. Transitions happen around V_{IH} and V_{IL} but in the transition region, a very high gain is desirable. Looking at the values we conclude the inverters

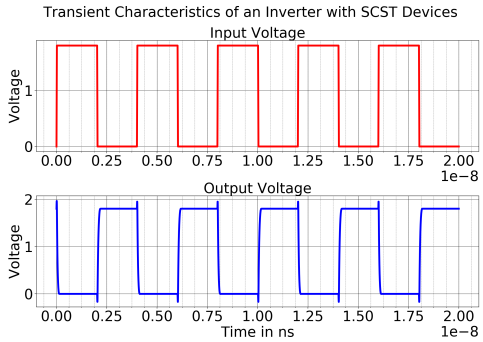
Table 3.3: Noise Margins of Inverter with different Devices

Device Technology	V_{OL}(V)	V_{IL}(V)	V_{IH}(V)	V_{OH}(V)	NM_H(V)	NM_L(V)
SCST	0.04	0.59	1.15	1.73	0.58	0.55
LCLT	0.04	0.61	1.2	1.72	0.52	0.57
SCLT	0.04	0.61	1.21	1.73	0.52	0.57
180nm PTM	0.15	0.50	0.91	1.68	0.77	0.35

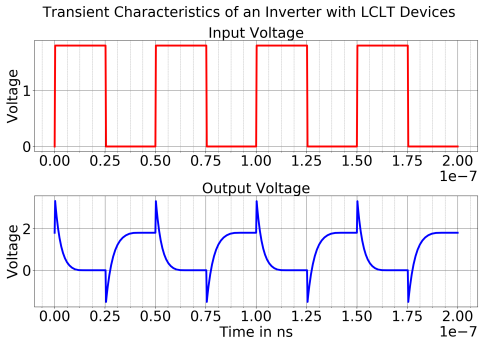
implemented with our devices have noise margins that are balanced as compared to the 180nm benchmark PTM technology. We know from figure 3.3d that the 180nm benchmark inverter is a skewed inverter. This happens because the NMOS is stronger. Mobility of electrons being more than the holes contributes to this behaviour.

Dynamic Behaviour of an Inverter

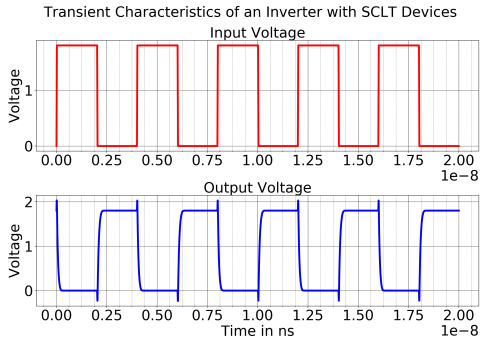
As a first order model, by looking at the schematic of the inverter in the figure 3.2, we can say that the transient analysis of the inverter will be dominated and dictated in large terms by the C_{LOAD} at the Output node of the inverter. The C_{LOAD} consists of the NMOS and the PMOS drain diffusion capacitances, interconnect capacitance to the next gate and the input capacitances of the fanout gates. We can say that the time required to switch the inverter to a high logic value will be determined by the time it takes to charge this C_{LOAD} through the PMOS Resistance R_P. So, the propagation delay for a low-to-high transition will be proportional to the product R_PC_L. Similarly for a high-to-low transition, the propagation delay will be proportional to the product R_NC_L [12] . To make faster transistors, in essence is to reduce the value of this Load Capacitance or reduce the non linear resistance of the transistor by tweaking the W/L ratio, which in our case translates to changing the number of tubes in the pull-up or the pull-down network. The propagation delay is analyzed from the transient response of the curve. The transient response of an inverter is obtained by giving a time varying voltage at the input of a CMOS inverter. Logic 1 at input will produce a logic 0 at the output and vice versa. To measure the propagation delay from a waveform, we calculate the time interval between the time the input voltage reaches 50% of V_{DD} to the time the output voltage reaches 50% of V_{DD}. We have plotted the transient response of the inverter circuit generated from all our devices as well as the 180nm technology we use for benchmarking in figure 3.4. Propagation delay is impacted by a number of factors viz. the load capacitance, the supply voltage and the number of tubes in the pull-up/pull-down network. High-to-Low propagation delay is denoted by t_{pHL} and Low-to-High delay is denoted by t_{pLH}. The average of the two delays gives us the total propagation delay of the inverter. We have assumed a load capacitance of 1fF in addition to the device capacitance obtained from the simplified model for our transient analysis calculations. Supply Voltage of 1.8V and 1 PMOS and 1 NMOS tube is also taken into account for calculation. We can conclude that SCST devices are the fastest devices as expected because of the less



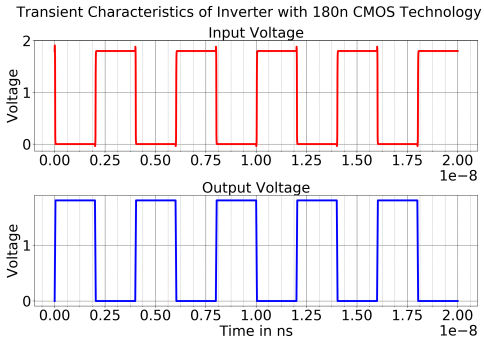
(a) Transient Characteristics for the SCST Devices



(b) Transient Characteristics for the LCLT Devices



(c) Transient Characteristics for the SCLT Devices



(d) Transient Characteristics for 180nm Benchmark Technology

Figure 3.4: Transient Characteristics of an Inverter.

Table 3.4: Summary of Inverter Transient Characteristics

Device Technology	t_{pLH}	t_{pHL}	t_p
SCST	38.94ps	32.56ps	35.75ps
LCLT	4.47ns	3.62ns	4.05ns
SCLT	59.25ps	53.21ps	56.23ps
180nm PTM	12.23ps	4.69ps	8.46ps

capacitance of the short channel and less resistance of the short terminals. LCLT Inverters are the slowest with propagation times in order of 4ns, due to the high device capacitance because of a longer geometry. SCLT as expected are between the SCST and the LCLT devices. The 180nm benchmark technology is the fastest out of all the simulations that were run. The H2L and L2H times confirm to our analysis from figure 3.3d that the inverter is skewed by a stronger NMOS leading to a smaller H2L delay as compared to a L2H delay. This subsection summarizes the CMOS Inverter for it's DC and Transient Operation.

3.3 CMOS NAND

:

The CMOS Nand is a universal gate whose output is low when both the inputs are high. It is one of major static CMOS Gates. To create a CMOS Nand gate, a pull-up and a pull-down network of transistors or tubes is created. The pull-up network consists of PMOS Nanowires whereas the pull-down network consists of NMOS Nanowires. The pull-down network has two transistors in series whereas the pull-up network has two transistors in parallel. Concluding from the construction of the gate we can say that there is only one input case where the output is low, when both the NMOS transistors in the pull down network are on. Intuitively, we can conclude that the DC Characteristics of a NAND Gate for all the different possibilities will be shifted to the right as compared to the VTC of an inverter. This implies the reluctancy of the output to switch down to a logic 0 level as is evident from the truth table which has 3 states where the output is high but only 1 where the output is low. We have explored a transient analysis response of the CMOS Nand Gate by looking at the plots from 4 different technologies in figure 3.6.

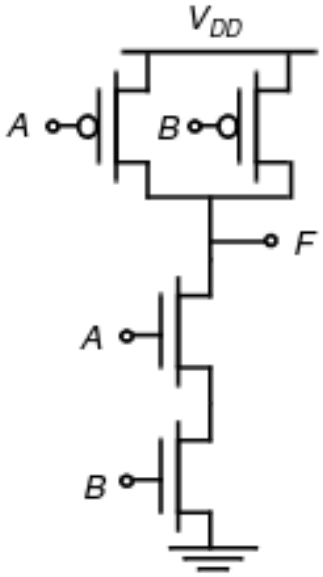
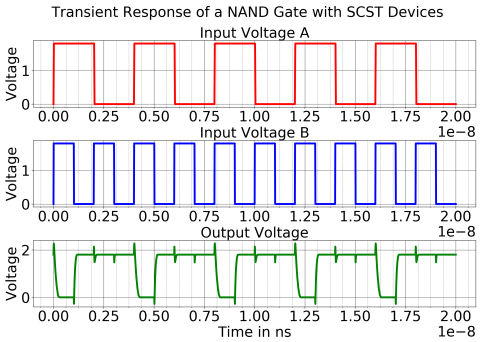


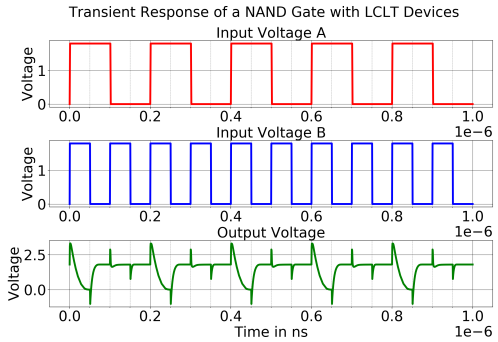
Figure 3.5: CMOS Nand Gate Schematic [6]

Table 3.5: Truth table of a CMOS NAND Gate

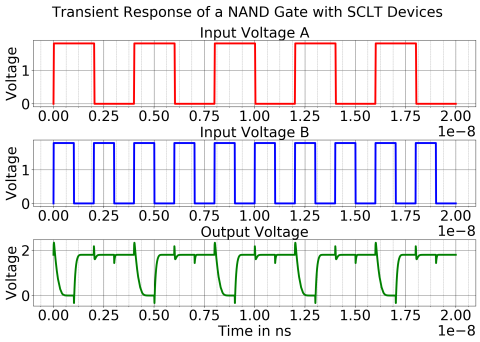
InputA	InputB	Output
0	0	1
0	1	1
1	0	1
1	1	0



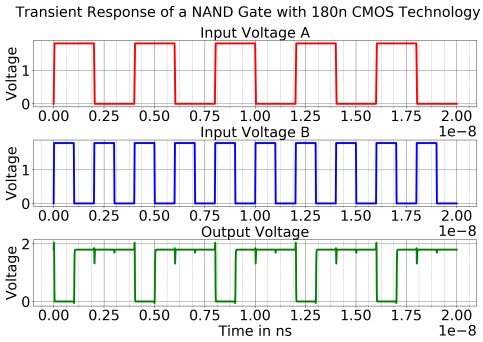
(a) Transient Characteristics for the SCST Devices



(b) Transient Characteristics for the LCLT Devices



(c) Transient Characteristics for the SCLT Devices



(d) Transient Characteristics for 180nm Benchmark Technology

Figure 3.6: Transient Characteristics of a CMOS NAND Gate.

The input A for the SCST, SCLT and the Benchmark simulation in figure 3.6 is a 4ns period wave, whereas the input B is a 2ns period wave. For LCLT devices, the input A is a 200ns period square wave and input B is a 100ns period wave. We have some time data for the Nand Gate propagation delay from our circuits as a function of the input pattern. We can conclude from the numbers in table 3.6 that our simulation results match our theoretical expectations. We observe that the H2L delay is much more than the L2H delay for our devices. We use an input pattern where any one of the inputs is fixed to a logic 1 level

Table 3.6: Summary of Important CMOS NAND Gate Delays

Device Technology	Input A	Input B	Output	t_{pLH}	t_{pHL}
SCST	1	$0 \rightarrow 1$	$1 \rightarrow 0$	-	90.05ps
SCST	1	$1 \rightarrow 0$	$0 \rightarrow 1$	41.86ps	-
LCLT	1	$0 \rightarrow 1$	$1 \rightarrow 0$	-	16.51ns
LCLT	1	$1 \rightarrow 0$	$0 \rightarrow 1$	5.14ns	-
SCLT	1	$0 \rightarrow 1$	$1 \rightarrow 0$	-	160ps
SCLT	1	$1 \rightarrow 0$	$0 \rightarrow 1$	64.27ps	-
180nm PTM	1	$0 \rightarrow 1$	$1 \rightarrow 0$	-	11.43ps
180nm PTM	1	$1 \rightarrow 0$	$0 \rightarrow 1$	17.23ps	-

and the other is transitioned from 0 to 1 or vice-versa and the delays are measured. When one input is fixed at 1, the intermediate capacitor between two NMOSes is also charged up following Elmore Delay model. When the other input now switches to logic 1, not only the output node but also the intermediate node has to be discharged to ground, thereby increasing the value of H2L delay.

3.4 CMOS NOR

:

The CMOS Nor is a universal gate whose output is high only when both the inputs are low. It is one of major static CMOS Gates. To create a CMOS Nor gate, a pull-up and a pull-down network of transistors or tubes is created. The pull-up network consists of PMOS Nanowires whereas the pull-down network consists of NMOS Nanowires. The pull-down network has two transistors in parallel whereas the pull-up network has two transistors in series. Concluding from the construction of the gate we can say that there is only one input case where the output is high, when both the PMOS transistors in the pull-up network are on. Intuitively, we can conclude that the DC Characteristics of a NOR Gate for all the different possibilities will be shifted to the left as compared to the VTC of an inverter. This implies the reluctancy of the output to switch to a logic 1 level as is evident from the truth table which has 3 states where the output is low but only 1 where the output is high. We have explored a transient analysis response of the CMOS Nor Gate by looking at the plots from 4 different technologies in figure 3.8.

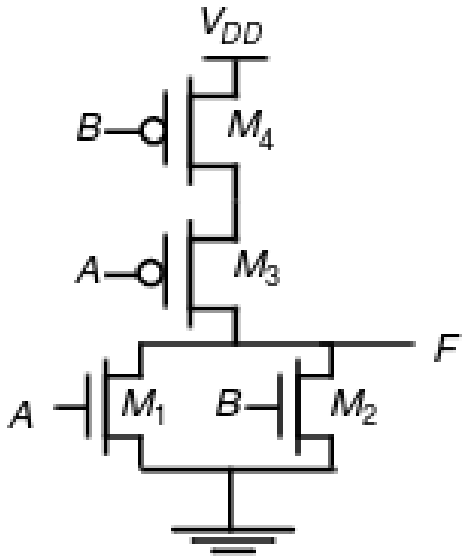
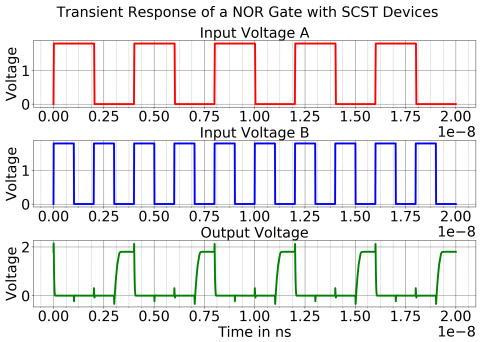


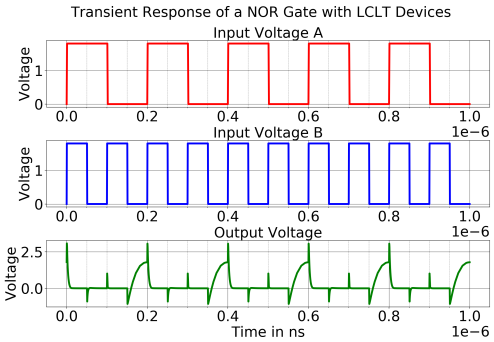
Figure 3.7: CMOS Nor Gate Schematic

Table 3.7: Truth table of a CMOS NOR Gate [6]

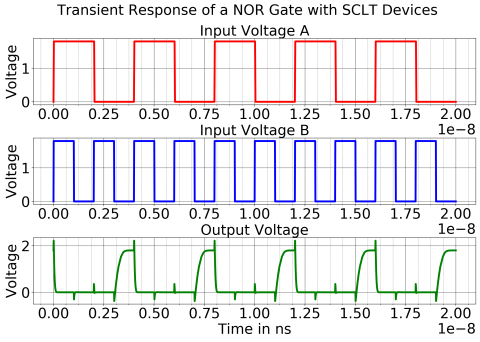
InputA	InputB	Output
0	0	1
0	1	0
1	0	0
1	1	0



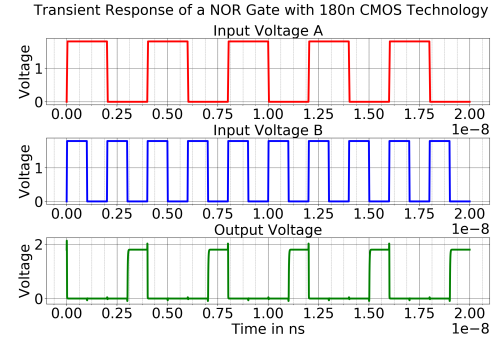
(a) Transient Characteristics for the SCST Devices



(b) Transient Characteristics for the LCLT Devices



(c) Transient Characteristics for the SCLT Devices



(d) Transient Characteristics for 180nm Benchmark Technology

Figure 3.8: Transient Characteristics of a CMOS NOR Gate.

The input A for the SCST, SCLT and the Benchmark simulation in figure 3.8 is a 4ns period wave, whereas the input B is a 2ns period wave. For LCLT devices, the input A is a 200ns period square wave and input B is a 100ns period wave. We have some time data for the Nor Gate propagation delay from our circuits as a function of the input pattern. We can conclude from the numbers in table 3.8 that our simulation results match our theoretical expectations. We observe that the L2L delay is much more than the H2L delay for our devices. We use an input pattern where any one of the inputs is fixed to a logic 0 level and

Table 3.8: Summary of Important CMOS NOR Gate Delays

Device Technology	Input A	Input B	Output	t_{pLH}	t_{pHL}
SCST	0	$0 \rightarrow 1$	$1 \rightarrow 0$	-	34.26ps
SCST	0	$1 \rightarrow 0$	$0 \rightarrow 1$	112.3ps	-
LCLT	0	$0 \rightarrow 1$	$1 \rightarrow 0$	-	4.03ns
LCLT	0	$1 \rightarrow 0$	$0 \rightarrow 1$	19.09ns	-
SCLT	0	$0 \rightarrow 1$	$1 \rightarrow 0$	-	64.27ps
SCLT	0	$1 \rightarrow 0$	$0 \rightarrow 1$	160ps	-
180nm PTM	0	$0 \rightarrow 1$	$1 \rightarrow 0$	-	57.12ps
180nm PTM	0	$1 \rightarrow 0$	$0 \rightarrow 1$	178.5ps	-

the other is transitioned from 0 to 1 or vice-versa and the delays are measured. When one input is fixed at 0, the intermediate capacitor between two PMOSes is also discharged up following Elmore Delay model. When the other input now switches to logic 0, not only the output node but also the intermediate node has to be charged to V_{DD}, thereby increasing the value of L2H delay.

3.5 Static CMOS Full Adder

A full adder is a 1 bit digital circuit that adds 3 inputs (A, B, C_{in}) and 2 outputs (S, C_{out}). A and B are operands whereas C_{in} is the carry from the previous stage. We implement a standard static CMOS Full adder using our devices to verify the functional correctness of the circuit. We have implemented the following circuit diagram to implement a full adder. The truth table is also shown in figure 3.9 We have simulated a full adder using each of

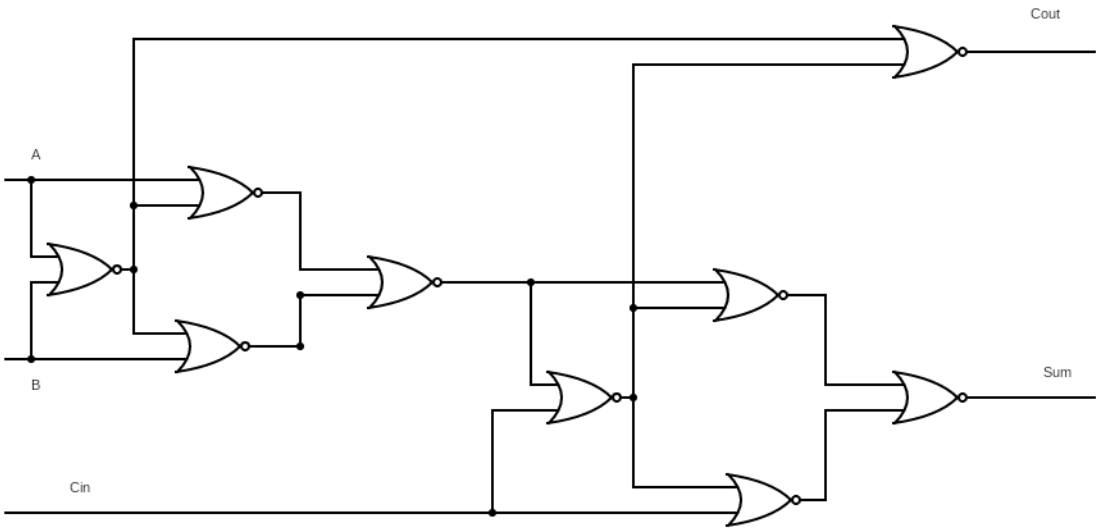
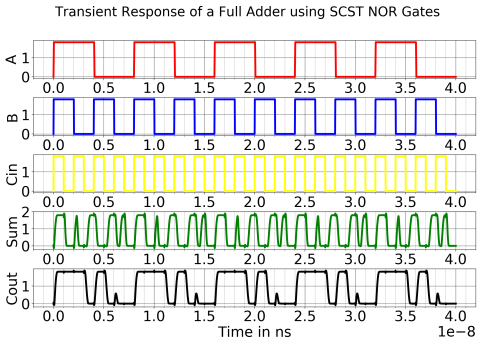


Figure 3.9: Full Adder using NOR Gates

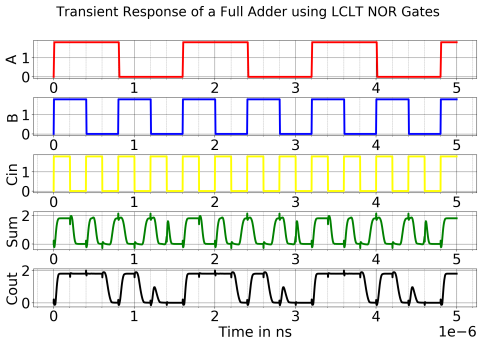
Table 3.9: Truth table of a 1-bit Full Adder

A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

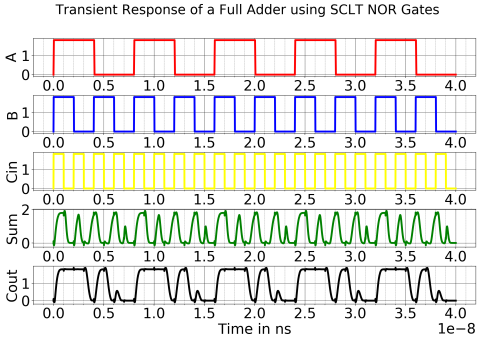
our technologies and the 180nm to get an idea of how the technologies compare.



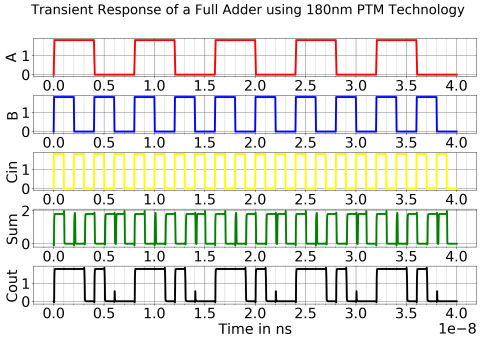
(a) Full Adder using SCST Devices



(b) Full Adder using LCLT Devices



(c) Full Adder using SCLT Devices



(d) Full Adder using 180nm PTM Technology

Figure 3.10: Transient Characteristics of a Full Adder using NOR Gates.

It can be observed that due to the delay of the NOR Gates involved in the construction of the full adder, there a lot of cases for the input transition where glitching happens at the output. For an input transition from 010 to 001, the Sum output should remain at 1 before and after the transition but the output momentarily tries to fall down to 0 and again rises to 1. This phenomenon is due to the critical path delay of the NOR Gates in the design.

3.6 Inverter with Fanout-4

The operation of the inverter with Fanout-4 is understood in this section. We know that the load capacitance at the output of the inverter has multiple capacitance components to it. It has the diffusion capacitance of the PMOS and the NMOS, the interconnect capacitance to the fanout gate and input capacitance of the fanout gate itself. The CMOS Inverter discussed in the previous sections just had 1fF of load capacitance at the output node. The Inverter with Fanout-4 in addition to the 1fF of load capacitance at the output also has 4 identical inverter gates being connected to the output of the concerned inverter. This additional gate capacitances will increase the propagation delays of an inverter, thereby reducing the speed of each stage. The schematic of an inverter with fanout-4 is shown in figure 3.11. The DC response of an inverter does not depend on the capacitance in the

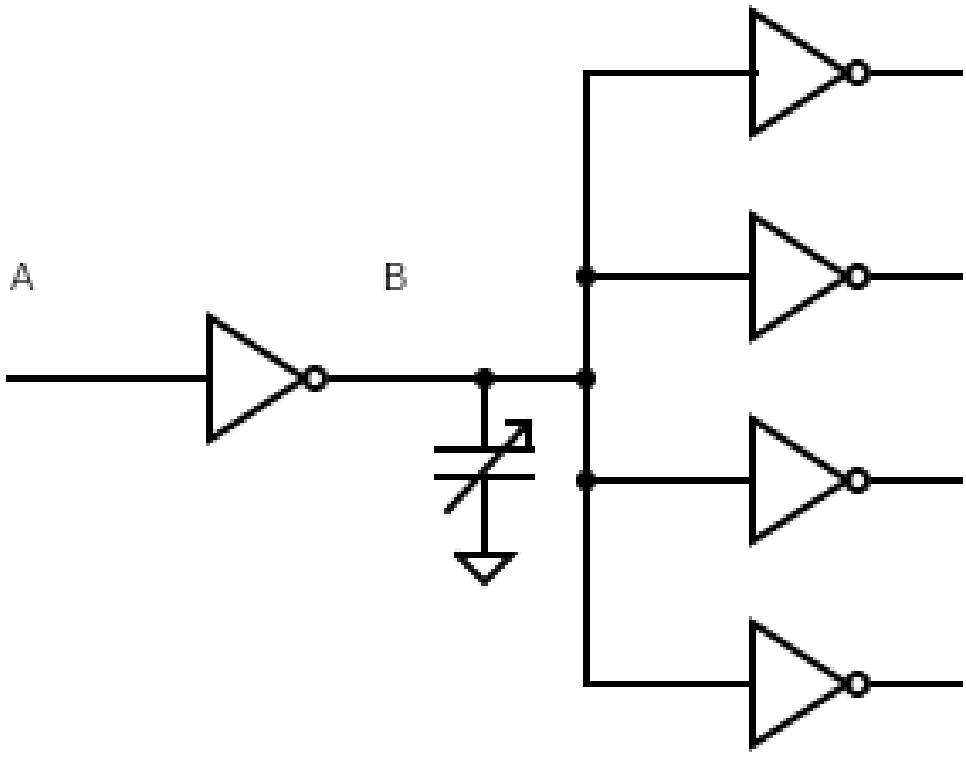
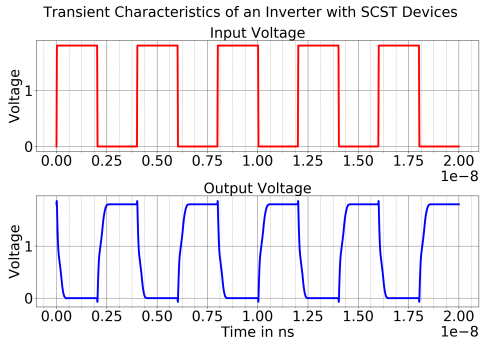


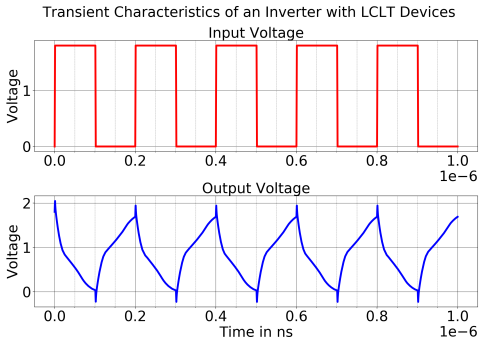
Figure 3.11: Inverter Gate with Fanout-4

circuit. Hence, we observe that the DC response of an inverter with Fanout-4 will also look like the plots of DC characteristics shown in figure 3.3. As for the transient response,

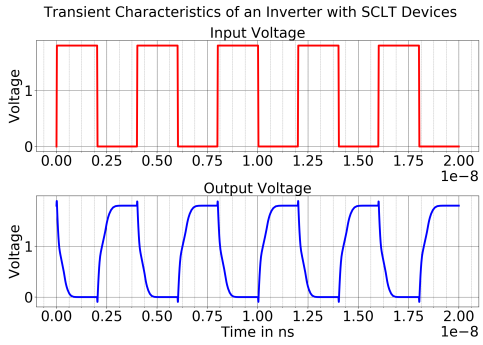
the nature of the curve remains the same but the response becomes much slower. We have plotted the responses of these circuits in figure 3.12. We also summarize the delay values in the table 3.10.



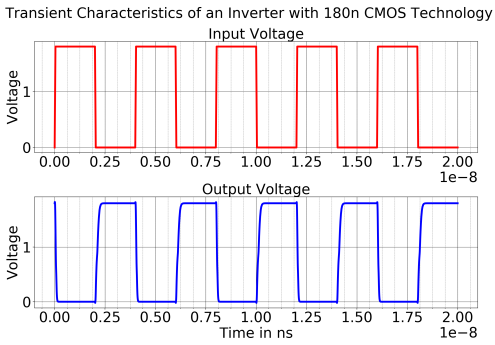
(a) A Fanout-4 Inverter using SCST Devices



(b) A Fanout-4 Inverter using LCLT Devices



(c) A Fanout-4 Inverter using SCLT Devices



(d) A Fanout-4 Inverter using 180nm PTM Technology

Figure 3.12: Transient Characteristics of an Fanout-4 Inverter

Table 3.10: Summary of Inverter Fanout-4 Transient Characteristics

Device Technology	t_{pLH}	t_{pHL}	t_p
SCST	122.3ps	86.04ps	104.17ps
LCLT	26.48ns	20.73ns	23.61ns
SCLT	182.30ps	155.10ps	168.7ps
180nm PTM	97.24ps	36.17ps	66.71ps

Looking at the numbers we can conclude that the High-to-Low and the Low-to-High delays have increased as compared to a standard CMOS Inverter with a load of just 1fF. This additional delay is attributed to the presence of 4 inverters at the output load of the concerned inverter.

3.7 3-Stage Ring Oscillator

A ring oscillator is a device composed of odd number of inverter stages, whose output is supposed to switch back and forth between two logic levels. It is just a chain of Inverters with the output of the last stage fed back to the first stage as its input. The output takes a finite amount of time to be asserted after the input has been asserted and this feedback of the last stage to the input causes the oscillation. The ring oscillator schematic is shown in the figure 3.13

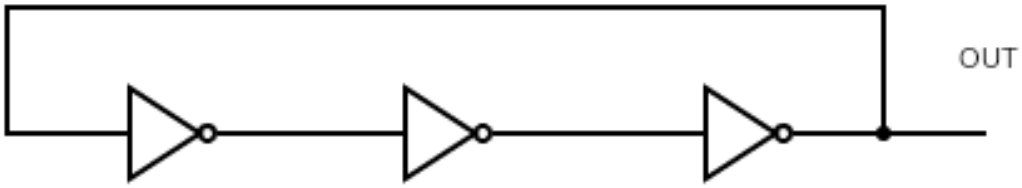


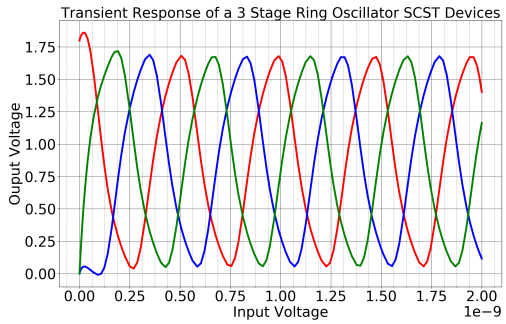
Figure 3.13: Ring Oscillator with 3 Inverter Stages

A good ring oscillator will require only power to operate. Above a certain supply voltage to the inverters, oscillations begin spontaneously. The frequency of operations can be increased by either using lesser number of stages or by reducing the inverter delay by making the supply voltage higher or the transistors bigger. All these eventually lead to less time to charge or discharge the capacitor and hence increased frequency. Current can only flow between the drain and the source of a transistor after the gate capacitance is charged. Thus, it can be said that the output of every inverter stage will only change a finite amount of time after the input has changed. Adding more stages will hence lead to increasing the chain delay and hence lowering the ring oscillator frequency. The ring oscillator frequency is given by the following equation.

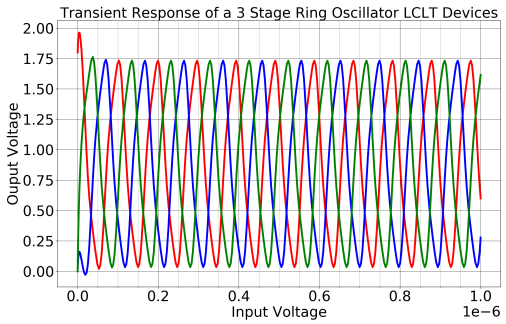
$$f = \frac{1}{2tn} \tag{3.7}$$

where n represents the number of inverter stages in a ring oscillator and t is the time delay for a single inverter. A ring oscillator is one of the first circuits to test out in new hardware

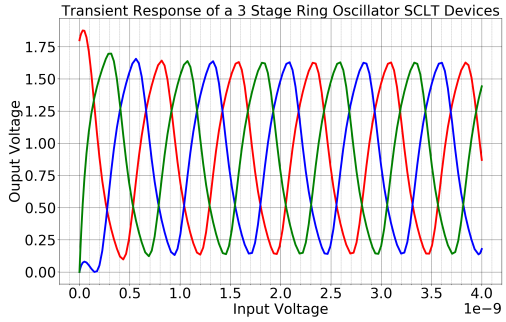
technology. This is one of the major reasons we decided to test a ring oscillator with our devices. The figure 3.14 shows the ring oscillator plots for each of our 3 devices and also the benchmark.



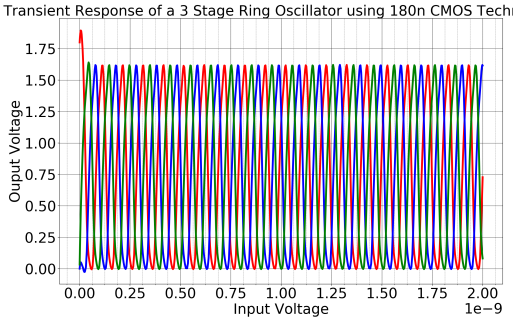
(a) A 3-Stage Ring Oscillator using SCST Devices



(b) A 3-Stage Ring Oscillator using LCLT Devices



(c) A 3-Stage Ring Oscillator using SCLT Devices



(d) A 3-Stage Ring Oscillator using 180nm PTM Technology

Figure 3.14: Transient Characteristics of a 3-stage Ring Oscillator

Table 3.11: Ring Oscillator Frequency

Device Technology	Ring Oscillator Frequency
SCST	2.08GHz
LCLT	10.31MHz
SCLT	1.315GHz
180nm PTM	9.885GHz

The ring oscillator frequencies have been obtained from simulation and measurement from the tool. We discuss the effect of load capacitance on the ring oscillator frequency in the later sections.

3.8 Effect of Interconnect Capacitance on the Performance of Digital Circuits

In this section, we discuss the effect of interconnect capacitance between our devices on digital circuit. The novel thing with respect to our large area flexible nanowires is that they are manufactured using printing rather than using the traditional lithographical methods. This allows us to vary the device sizes depending on the printer resolution. We start from Long Channel Long Terminal (LCLT) devices and then reducing the channel length to reach Short Channel Long Terminal (SCLT) devices and eventually reaching the fastest Short Channel Short Terminal (SCST) devices. The roadmap from LCLT $\rightarrow$ SCLT $\rightarrow$ SCST requires some considerable advances in material science and the printing technologies to manufacture the nanowires at low temperatures than lithography. Along with the device sizes, what printing also allows to be controlled is the distance between the 2 devices. LCLT devices can easily be printed with the interconnect distances of the order of 100μm by simply drop casting a solution of transistors over a substrate. With advanced material science techniques like blade coating, this distance can be bought down 100 times to around 1μm. Length of the interconnect between two devices plays a major role in deciding the load capacitance of the circuit and subsequently the performance of the circuit. We assume a standard Fanout-1 inverter with a variable load capacitance for a host of calculations and analysis with the length of the interconnect vs the performance and the energy of the circuits. The figure 3.15 shown below is used for the analysis. We lump the capacitance of 5 aspects into the output load capacitance. They are as follows:

- Parallel Plate Capacitance between NMOS and PMOS Nanowires of the Inverter.
- Fringe Field Capacitance of the interconnect between NMOS and PMOS Nanowires of the Inverter.
- Parallel Plate Capacitance of the interconnect between the 2 inverters.
- Fringe Field Capacitance of the interconnect between the 2 inverters.

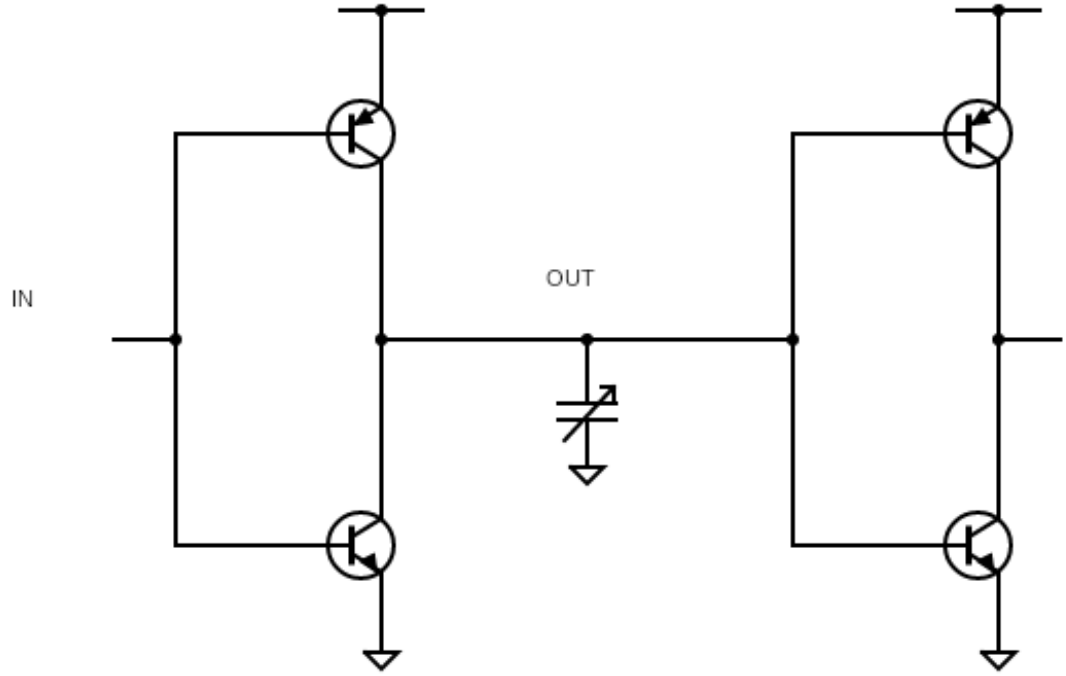


Figure 3.15: Fanout-1 Inverter with Variable Load Capacitance

- Coupling Capacitance of the interconnect net to its neighbouring net.

All the capacitance values are determined by the product of the capacitance per unit length with the total length. The Parallel component is dictated by the geometry of the interconnect.[6] [12] The fringe field model is a non-linear model of the capacitance to account for the electric field lines going out of the conductor. The interconnect fringe field lines have been shown in figure 3.16. The Parallel Plate Component is given by the following equation:

$$C = \frac{\epsilon_{\text{OX}} w l}{X_{\text{OX}}} \tag{3.8}$$

where ϵ_{OX} stands for the dielectric constant of the oxide, l for the interconnect length and X_{OX} denotes the thickness of the oxide. But this equation ignores the fringe field component of the capacitance contributed by the electric field lines shown in 3.16. So we use a

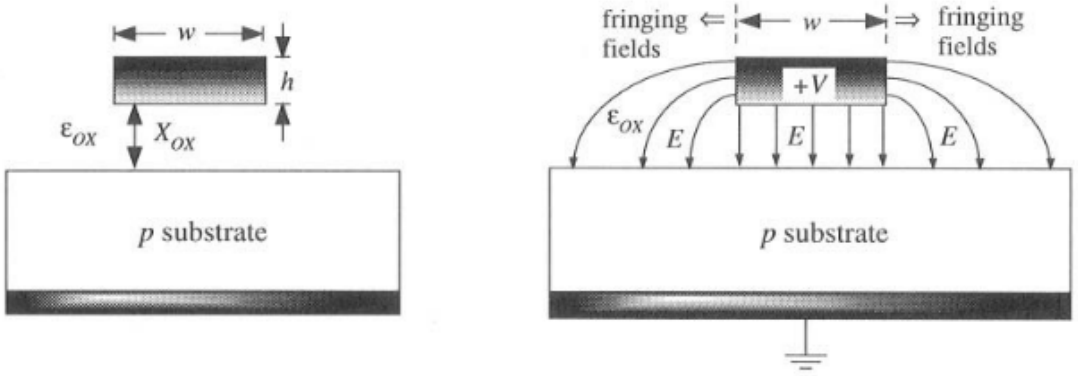


Figure 3.16: Parallel Plate and Fringe Field Capacitance

modified version of equation 3.8 to give equation 3.9

$$C = \epsilon_{\text{OX}}[1.15(\frac{w}{X_{\text{OX}}}) + 2.8(\frac{h}{X_{\text{OX}}})^{0.222}]F/cm \tag{3.9}$$

The first term in the equatin stands for the parallel plate component. It's been accounted by a factor of 15% to consider the fringing fields originating from the bottom plate while the second term in the equation above contributes to the fringing field originating from the side with a interconnect of height h. In modern sub-micron technology nodes, width w has become smaller than height h leading to an increased contribution the fringing fields. We assume that our interconnects are printed on a glass substrate with a thickness of 1000nm having a dielectric constant ϵ_{OX} value of 4. We assume the thickness and the width of the interconnect line to be around 1μm. The length is variable from 1μm to 100μm. The value of the capacitance is plotted versus interconnect length as the distance increases. This capacitance curve yields the value of 27.98fF at a interconnect distance of 1μm and a value of 2.798pF at a distance of 100μm. We use this capacitive array as an input to the spectre simulator as a value of the variable load capacitance and plot the propagation delay values as a function of the interconnect capacitance. We can see from the figure 3.17 that as the length increases the capacitance increases as the two are related by the equation 3.9. We stimulate circuit in figure 3.15 with a time varying response such that the capacitance is

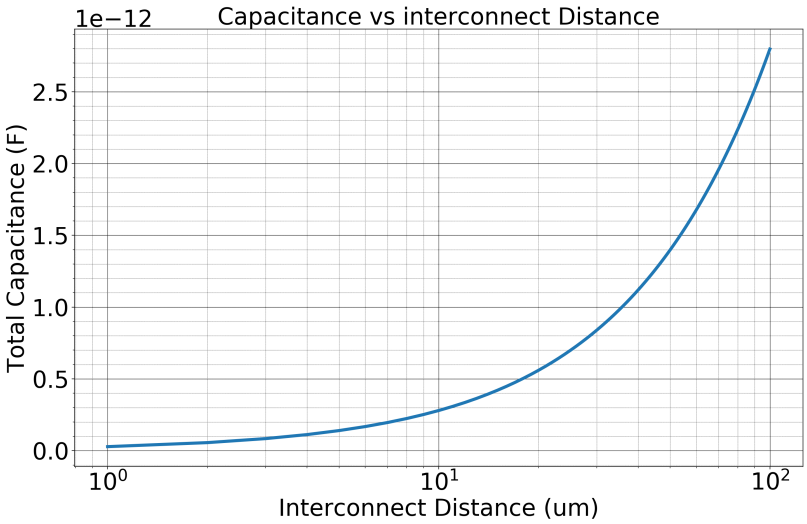
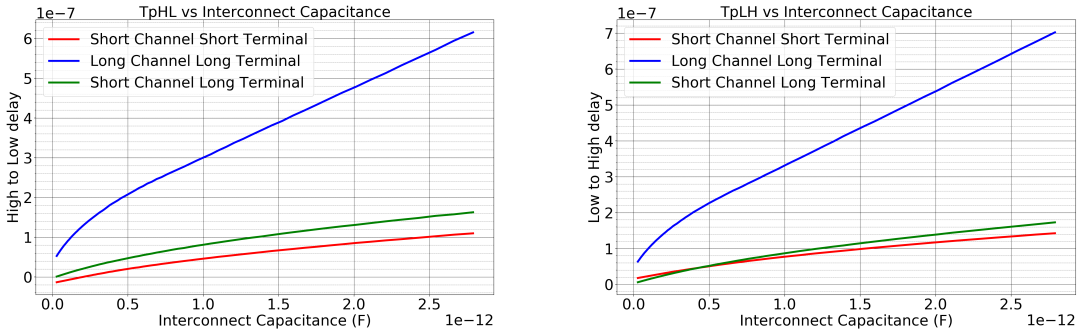


Figure 3.17: Capacitance vs Interconnect Length

varying with length and plot the high-to-low and the low-to-high propagation delay of the inverter. It is observed from these plots that the High-to-Low propagation delay for all the devices starts at a particular value. As the capacitance increases, the delay value tries to



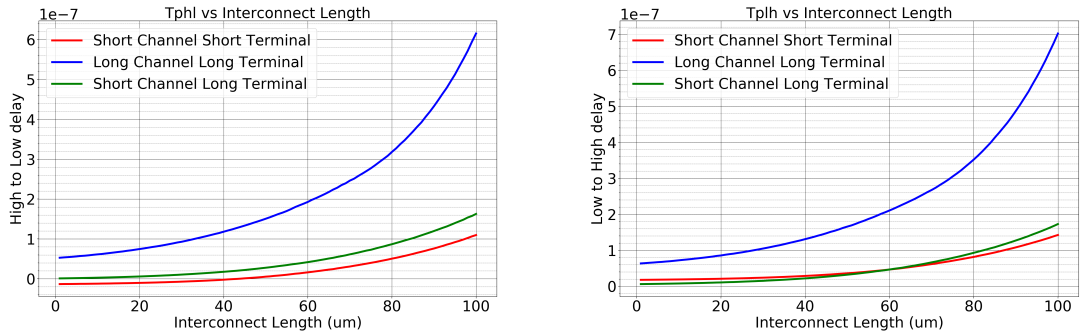
(a) High-to-Low Delay vs Interconnect Capacitance

(b) Low-to-High Delay vs Interconnect Capacitance

Figure 3.18: Propagation Delay vs Interconnect Capacitance

stay within minimal increase to the first value, after which it rises very fast. Eventually the delay is of the order of a few tens of microseconds for a LCLT device and around 0.1-1μs for the Short Channel devices. Similar behaviour is observed for the Low-to-High delay

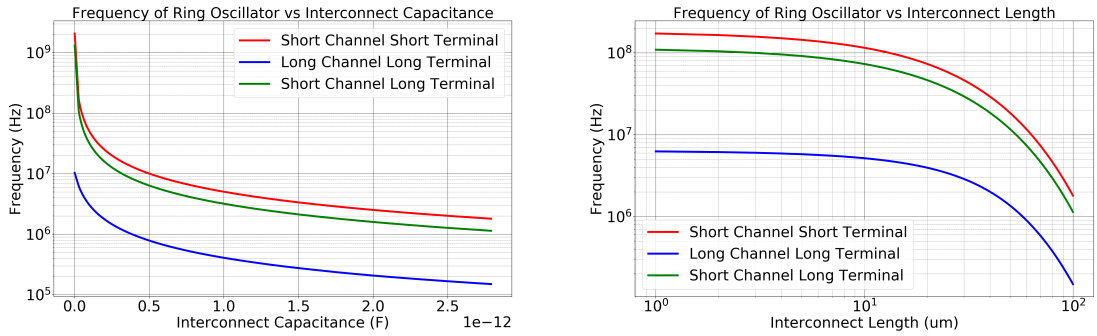
as well albeit the Low-to-High delay is traditionally higher than the High-to-Low delay for a given capacitance value. The corresponding delay plots have also been plotted as a function of the interconnect length in 3.19. We now explore the value of this variable



(a) High-to-Low Delay vs Interconnect Length **(b)** Low-to-High Delay vs Interconnect Length

Figure 3.19: Propagation Delay vs Interconnect Length

capacitance on the frequency of a 3-stage ring oscillator circuit as discussed before. The ring oscillator being one of the first digital circuits to be tested makes it mandatory for us to analyze the interconnect effects on the frequency. We observe that the ring oscillator



(a) Frequency vs Interconnect Capacitance **(b)** Frequency vs Interconnect Length

Figure 3.20: Frequency of a 3-Stage Ring Oscillator as a function of Interconnect Capacitance and Length

frequency starts out at a couple of GHz for the shortest device and reduces to a few hundred

MHz at an interconnect distance of around 100μm. Even with the LCLT devices, we can see that the frequency varies from a few hundred MHz at 1μm to a couple at 100. The increasing interconnect distance leads to a single inverter stage taking more time to charge or discharge the output capacitance, thereby reducing the overall ring oscillator delay and hence the frequency.

3.9 6-T SRAM Cell

Any new hardware technology is developed for sustaining advancements in Logic and Memory. We analyzed the performance of a traditional 6T SRAM Bitcell using Our SCST devices. The 6-T SRAM cell is a 1-bit memory storage element. It works on the principle that coupled inverters can store data. So, 6-T SRAM Cell consists of cross coupled inverters to store the data and access transistors on both the left and the right side to read or write the data. SRAM is a volatile memory in the sense that when the memory is not powered, the data stored inside a bitcell is lost. Word line and the access transistors are used to write the bitline data into the cell. A key figure of merit for an SRAM cell is its static noise margin (SNM). It can be extracted by nesting the largest possible square in the two voltage transfer curves (VTC) of the involved CMOS inverters, as seen in Figure . The SNM is defined as the side-length of the square, given in volts. When an external DC noise is larger than the SNM, the state of the SRAM cell can change and data is lost. SRAM Circuit Diagram is shown in figure 3.21. The Static Noise Margin Butterfly Curves for all

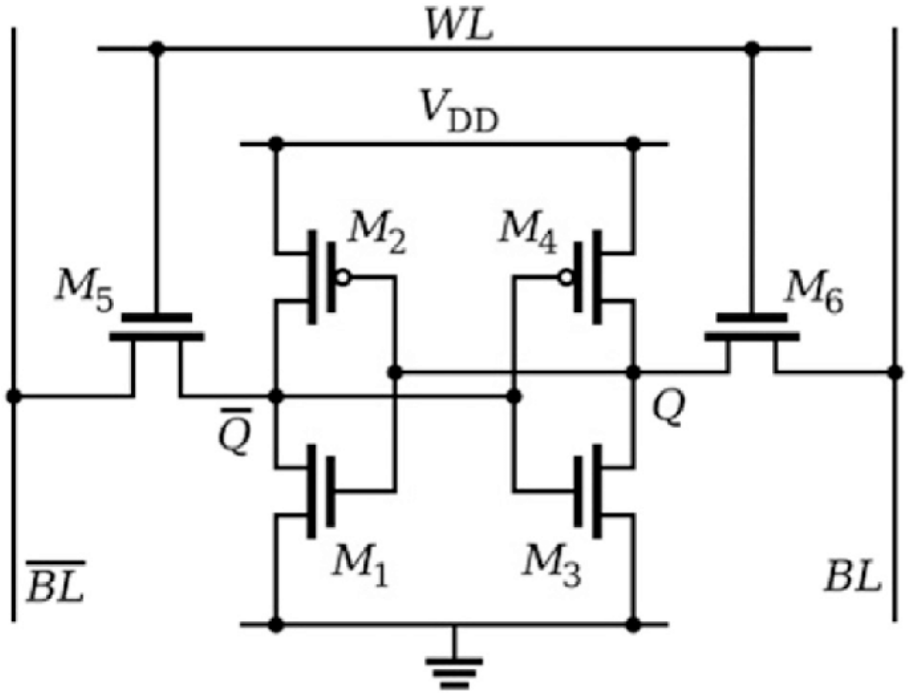


Figure 3.21: SRAM 6T Cell

our three devices are overlayed on top of each other for a comparative analysis as shown in figure 3.22. The simulation conditions for the plot in 3.22 are as follows:

- WL: Word line is a square pulse of 4ns oscillating from 0 to 1.8V.
- BL: Bit line is a square pulse of 2ns oscillating from 0 to 1.8V.
- BL_b: Bit line bar is a square pulse of 2ns oscillating from 1.8 to 0V.
- Vdd: DC Supply Voltage of 1.8V.

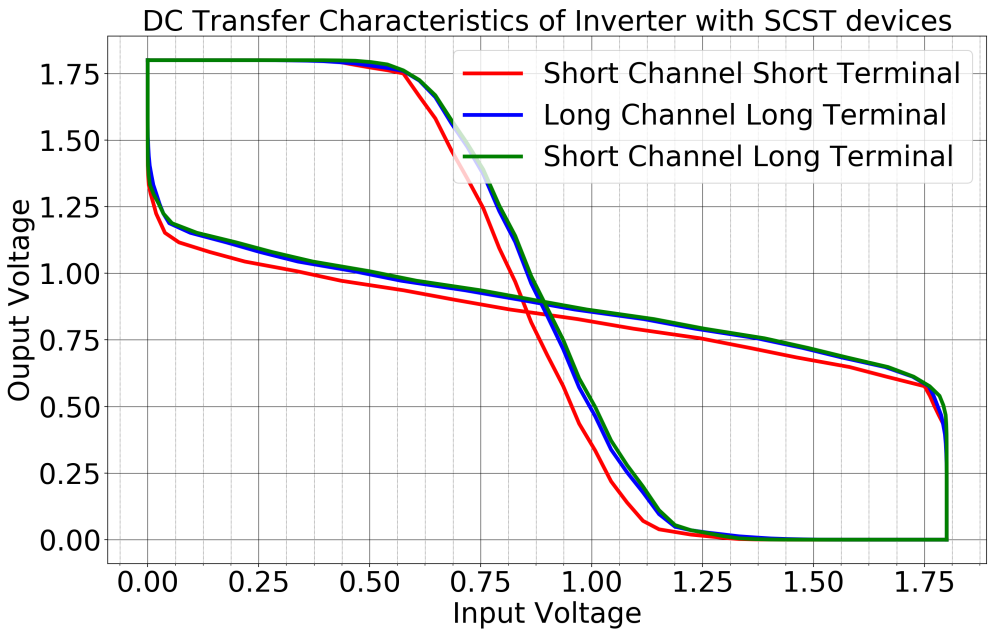


Figure 3.22: SRAM Static Noise Margin Characterization

It can be shown from the figure that the longest side of the square that can be fit in the butterfly is around 0.7 and hence SNM is around 0.7V.

CHAPTER 4
CONCLUSION

This section serves as the conclusion for the thesis. Introduction of this thesis starts out with describing the need for Gate all around devices. Simple operations of NMOS and PMOS Transistors are explained. Three regions of operation are delineated where each region has their own current characteristics depending on the voltage applied at the gate source junction and the drain source junction. The device geometries have been explored in much larger detail. Perfectly self aligned gate stacks have been designed, Since, the gate stacks are perfectly self-aligned, junction capacitance of the source and the drain coupled with the gate plays a major role in deciding the device capacitance. A non-self aligned gate stack will have the overlap capacitance play a major role in the devices which can lead to slower devices. The need and the requirement of ideal of Large Area Electronics has been explained. Short Channel effects and it's negative effect on the device threshold voltage is one of the major problems with the technology node scaling down nowadays. The Industry transition from Planar MOSFETs to Double Gated MOSFETs to State of the art FinFETs has helped us get rid of a lot of problems that were persistent in the technology. High-K Metal gates helped resolve the problem associated with gate leakage that arises due to tunnelling. Gate all Around devices give a greater control of the charge in the channel and allow us to retain the electrostatics of the device thus helping design better devices and eventually circuits.

Devices section explains the device in detail. The meshing densities of the devices play a major role in the interplay between the accuracy and the runtime of the device simulation. The physical models to integrate for the simulation have also been explored in detail. Coulumb Scattering, Surface Roughness Scattering, Phonnon Scattering and recombination models have been introduced in this section. Once, the device has been simulated, we

get Voltage-Current plots of the PMOS and the NMOS. This plots are explored in detail by analyzing parameters like the Threshold Voltage, the On Current and the Off-Current of the device. One of the major hindrances while doing the devices was selecting the PMOS and the NMOS pair with the right workfunction. The workfunction of the devices was sweeped from around 4.5-5eV to get a shif in the threshold voltage of the device. Higher the work-function, more is the threshold voltage of the device, hence it takes more time to turn on the device. Evaluations yield that the devices are nearly ideal with closer to a 130nm CMOS Technology devices. They have very high On-Off current ratios of the order of 10×10^5 and a NMOS to PMOS On-Current ratio of around 2-4 so that it does not make either of the devices more skewed. We evalauated our devices on a supply voltage of 1.8V, as we benchmarked the technology to a 180nm CMOS technology that has a supply voltage of 1.8V with a device threshold voltage of around 0.4-0.6V.

After the device selection has been concluded, we implement the circuit research in the SPECTRE Simulator. The Figure of Merit circuits have been tested for their functional verification and performance. The Simulation Infrastructure was one of the major issues to implement. It has to work right from understanding the device simulation log files, parsing them, create the netlist, simulate them in the right environment. Different circuits have their own nitigrities that come into interplay when given a specific input voltage. Device Capacitance for the individual devices can be extracted either from the device simulator or some analytical method. Our devices being cylindrical Gate All Around structures make it easier for us to use an analytical model to get to a value of device capacitance.

Device Capacitance is essential to simulate a transient response of the circuit. High to Low and Low to High switching speeds are a major figure of merit for any digital logic circuit. Switching speeds depends on the device capacitances as well as the capacitances at the output node of these circuits. Higher the load capacitance, more the time it takes for the circuit to charge or discharge this output node and hence, the low-to-high propagation delay will also be more. Performance of different circuits has been evaluated and hence

put forward in the circuits section. The effect of interconnects has been explored in greater detail in the devices section.

Our evaluations of this work show that the standalone devices are better than the 180nm CMOS Technology devices. They have better On-Currents, lesser Off-Currents and hence better On-OFF ratios, which can be attributed to the Gate All Around architecture. The circuits also functionally work the way they are expected to with the DC response of the inverter very close to the ideal circuit and the transient response showing full swings. The simulation of thhe 180nm Benchmark CMOS Technology also aids in an apples to apples comparison. The addition of interconnects includes the calculation of parasitic resistances and the capacitances. The parasitic resistance can be of approximated to a value of 0 since, we are dealing with large area electronics with larger interconnects between them. On the other hand, capacitance becomes of paramount importance when dealing with large area electronics. Adding interconnects to our devices that vary with length, we can say that even though the device standalone is comparable to a 130nm CMOS Technology, the system as a whole approaches the performance of a 180nm CMOS System.

The simulation methodology combined with the fabrication techniques involved make this work more suitable for large area electronics. We can manufacture devices on a large scale but also simultaneously achieve a very good performance specifications. This is one of the first works that implements and models devices used for wireless sensor nodes that are not built by a top-down photolithography process. We can say that overall the performance of the devices was much better than the corresponding CMOS Technology due to the Gate All Around structure and the cylindrical geometry. Future work can focus on including more complex device simulation models like analyzing defects or traps in the oxide above the channel and simulating more complex circuits. This work which lays out the roadmap of the devices from Long Channel Long Terminal to Short Channel Long Terminal to Short Channel Short Terminal certainly serves as a stepping stone for future research in the field of High Performance Large Area electronics.

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